

Department of Electrical Engineering

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ELEG3923 Microprocessor Midterm Review

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CH.0 AND CH.1 PRELIMINARIES

- **Concepts**
 - Microprocessor v.s. Microcontroller
 - Embedded systems
- **Numbering system**
 - Conversions between: decimal, binary, hexadecimal
 - Operations: addition, 2's complement
- **Basic digital logics**
- **Computer operations**
 - Bit, nibble, byte, word
 - kilo-, mega-, giga-
 - Computer structure: CPU, memory, I/O ports, bus (address, data, control)
 - Address bus: bus width v.s. memory space
 - Inside CPU: ALU, registers, instruction register, instruction decoder, program counter.

CH.2 ASSEMBLY PROGRAMMING

- **Assembly language**

- [label:] mnemonic [operands] [;comments]
- Assembler → (Obj, lst) → linker → (absolute file) → Obj 2 Hex → (Hex)
 - The contents of each file (e.g. obj: binary opcode, lst: a text file with a combination of source code, opcode, and addresses)

- **Directives**

- ORG, EQU, DB, END

- **ROM Space**

- PC (16-bit),
- starting address and ending address of ROM with different size

- **PSW**

- CY, AC, RS1, RS0, OV, P

CH.2 ASSEMBLY PROGRAMMING

- **Register bank and stack**

- RAM (128 bytes): register banks (32 bytes, 00 – 1F), bit-addressable (16 bytes, 20 – 2F), scratch pad (80 bytes, 30 – 7F)
 - Given address range, calculate memory size
- Register banks
 - RS1 and RS0
 - Default: register bank 0
- Stack
 - SP register
 - Default stack

- **Instructions**

- MOV, ADD, SETB, CLR, PUSH, POP

CH.3 JUMP, LOOP, CALL

- **Jump**

- Conditional jump
 - DJNZ, JZ, JNZ, JNC
 - All of them are short jumps
- Unconditional jump
 - SJMP, LJMP
- Range of short jump and long jump
- Calculation of offset

- **Call instructions**

- Subroutine
- LCALL, ACALL (address range)
- Format of subroutine (RET)
- Call instruction and stack

- **Delay**

- Clock frequency, clock period, machine cycle, # machine cycles/instruction
- Delay calculation (# of machine cycles/instruction will be provided to you during test).

CH.4 I/O PORTS

- **I/O Ports**
 - P0 (pull-up resistors), P1, P2, P3
 - Write to port
 - Read from port (input mode)
- **I/O port Bit manipulation**
 - Px.y
 - Conditional jump
 - JB, JNB, JBC
 - Be able to write programs to perform certain operations based on the value of a port bit (examples)
 - Port structure
 - Latch
 - Read-write-modify
 - CPL, XRL

CH.8 HARDWARE

- **Pin description**
 - Functions of the pin:
 - Vcc, GND, XTAL1, XTAL2, RST, EA, PSEN, ALE
 - How to connect XTAL
 - How to connect RST
- **Intel HEX file**
 - Be able to analyze the format of an Intel Hex file

CH.5 ADDRESSING MODE

- **Immediate**
 - MOV A, #0F3
 - Special cases: Directive, label, ASCII
- **Register**
 - MOV A, R0
 - DPTR (16-bit)
- **Direct addressing mode (RAM)**
 - MOV A, 30H
- **Register indirect addressing mode (RAM)**
 - MOV A, @R0
 - Access a group of data through loop
- **Indexed mode (ROM)**
 - MOVC A, @A+DPTR

CH.5 ADDRESSING MODE

- **Bit addressable memory**
 - Bit address v.s. byte address
 - BIT directive
- **Extra 128 bytes of RAM**
 - Share the same address space as SFRs (physically different from SFR)
 - SFR: direct addressing mode or register name
 - Extra 128 bytes of RAM: register indirect