

Department of Electrical Engineering

University of Arkansas



# **ELEG3923 Microprocessor Ch.8 Hardware Connection**

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# OUTLINE

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- **Pin description**
- **DS89C4x0 Trainer**
- **Intel Hex file**

# PIN: LAYOUT

- **Pin layout**

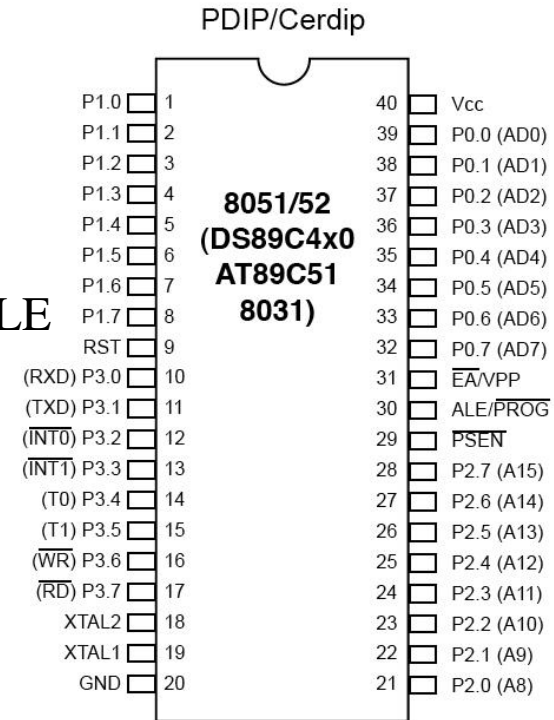
- A total of 40 pins
- 32 pins are used for I/O ports (8 pins/port, 4 ports)
- The remaining 8 pins
  - $V_{cc}$ , GND, XTAL1, XTAL2, RST,  $\overline{EA}$ ,  $\overline{PSEN}$ , ALE

- **Vcc**

- Pin 40. Provide supply voltage to the chip.
- Voltage source is +5V.

- **GND**

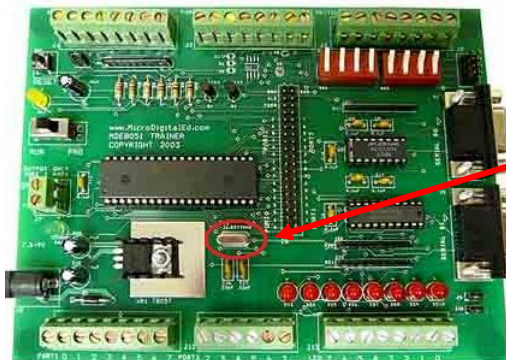
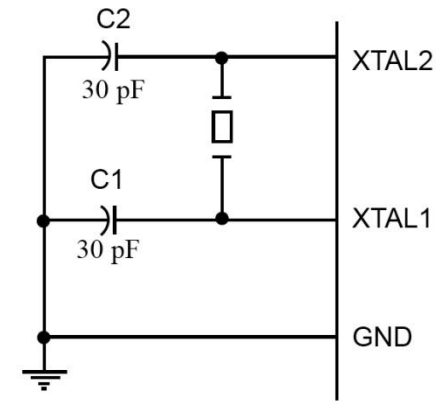
- Pin 20. Ground



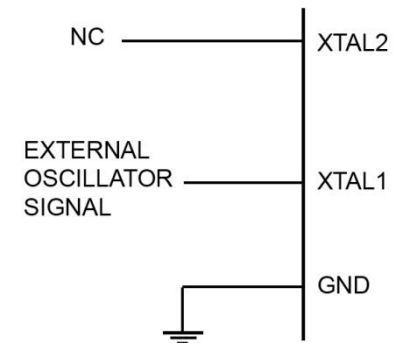
# PIN: XTAL1 AND XTAL2

## • XTAL1 and XTAL2

- Provide external clock to the 8051 (input pins)
- Configuration 1 (most common):
  - Connect to a quartz crystal oscillator
  - Crystal oscillator can generate square waveform at a fixed frequency (e.g. 11.0592 MHz)
  - Different 8051 chips have different speed ratings
    - E.g. a 12-MHz chip can only be connected to a crystal oscillator with frequency 12 MHz or lower.
  - We can observe the clock with an oscilloscope on XTAL2 pin
- Configuration 2:
  - Connect it to an external TTL oscillator (e.g. a clock signal generated by a function generator)
  - Only XTAL1 is used, XTAL2 is left unconnected (NC: not connected)



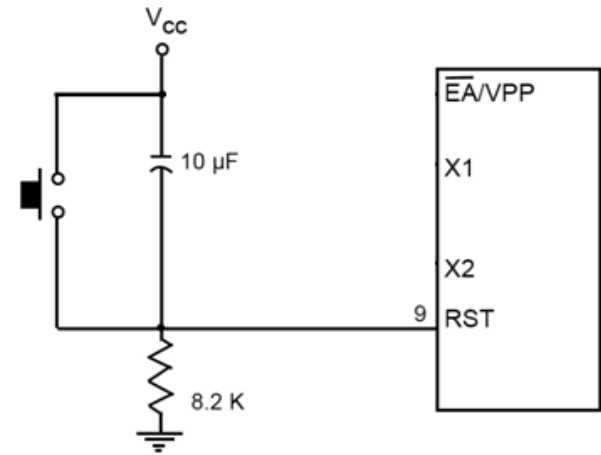
crystal oscillator



# PIN: RST

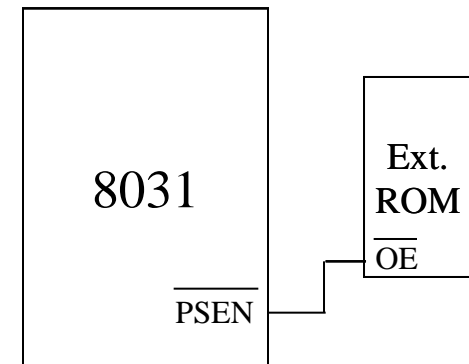
- **RST**

- Reset (input pin)
- Active high: upon applying a high pulse to the pin, the uC will reset and terminate all activities.
  - Normally it's value is low so uC can work normally.
  - In order for it too be effective, the high pulse must be high for a minimum of 2 machine cycles.
- Reset by switch
  - When SW is open, RST is low
  - When SW is closed, RST is high
  - When SW is released, RST is low
  - reset.
- Power on reset
  - At the instant of power on, RST is high
  - After a while, the capacitor will be fully charged
  - In steady state, RST is low.



# PIN: $\overline{EA}$ , $\overline{PSN}$ , AND ALE

- **8031**
  - A simplified version of 8051, it doesn't have built in ROM or RAM
  - It needs to be connected to external ROM and RAM through  $\overline{EA}$ ,  $\overline{PSN}$ , and ALE
- **$\overline{EA}$** 
  - External access (input pin): indicate whether there is an external ROM
  - Active low: it's effective when the voltage is low
  - If it is connected to ground  $\rightarrow$  there is external ROM
  - If it is connected to  $V_{cc}$   $\rightarrow$  there is no external ROM
- **$\overline{PSEN}$** 
  - Program store enable (output pin, similar to read)
  - If external ROM is connected to the uC, this pin is connected to the OE (output enable) pin of the ROM to enable the output of the ROM.
  - Active low: it's effective when the voltage is low
- **ALE**
  - Address latch enable (output pin)
  - Port 0 is used as both address bus and data bus for external RAM
  - If it's high, then P0 is used as address bus; if it's low, then P0 is used as data bus.



# PIN: DEFAULT VALUES

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- The default value of some 8051 registers upon reset

<b>Register</b>	<b>Reset Value (hex)</b>
PC	0000
DPTR	0000
ACC	00
PSW	00
SP	07
B	00
P0-P3	FF

- Machine cycle and crystal frequency

<b>Chip (Maker)</b>	<b>Clocks per Machine Cycle</b>
AT89C51/52 (Atmel)	12
P89C54X2 (Phillips)	6
DS5000 (Dallas Semiconductor)	4
DS89C4x0 (Dallas Semiconductor)	1

# OUTLINE

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- Pin description
- **DS89C4x0 HardwareTrainer**
- Intel Hex file

# HARDWARE: KEY FEATURES

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- **Key features of DS89C4x0**

- On chip flash ROM
  - DS89C420/30: 16KB
  - DS89C440: 32KB
  - DS89C450: 64KB
- High speed
  - 1 clock per machine cycle
  - DC to 33 MHz operation (it can be connected to a crystal with freq. up to 33KMHz)
- 256 bytes RAM
- Two full duplex serial ports
- 13 interrupt sources (6 external) with 5 level of interrupt priority
- Programmable watchdog timer.

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# INTEL HEX FILE

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- **Format of Intel hex file**

- Each line starts with a colon
- CC: the number of bytes in this line, the maximum value of 10H
- AAAA: a 16-bit address indicating where the first byte of the line should be stored in ROM
- TT: type. If TT=00, then this is not the last line; if TT=01, this is the last line.
- DD...DDD: the real data or code to be stored in ROM
- SS: checksum for everything in the line to make sure there is no error.
- It always ends with FF.

```

:CC  AAAA  TT      DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD  SS
:10  0000  00      75805575905575A0557DFA111C7580AA  9F
:10  0010  00      7590AA75A0AA7DFA111C80E47C237B4F  01
:07  0020  00      DBFEDCFADDF622  35
:00  0000  01      FF

```

