

# Motivation to use Asynchronous Circuits

- Asynchronous advantages vs. synchronous
  - no global clock
  - lower power
  - less noise
  - less EMI
- ITRS predicts likely shift from synchronous to asynchronous design styles
  - increase circuit robustness
  - decrease power
  - alleviate many clock-related issues
- ITRS predicts that asynchronous circuits will account for 19% of chip area within the next 5 years, and 30% of chip area within the next 10 years

# Comparison of Asynchronous Paradigms

## Bounded-Delay

- Substantial Glitch Power
- Worse-Case Performance
- Substantial Timing Analysis Required
  - bundled data convention
  - datapath delay must be matched in control path
- Micropipelines is best known example

## Delay-Insensitive

- Glitch Free
- Average-Case Performance
- Correct-by-Construction
  - multi-rail signals
  - completion detection
- Additional Advantages
  - very robust
    - tolerate process variations
    - tolerate power supply variations
    - tolerate vast temperature variations
  - design reuse is straightforward
  - easy to interface multi-rate circuits
  - reduced crosstalk

# Comparison of Delay-Insensitive Paradigms

- Precharge Half-Buffer (PCHB) logic family
  - dynamic logic
  - synthesis performed at transistor-level
  - uses non-standard EDA tools
- Phased-Logic
  - transforms synchronous circuit to delay-insensitive
  - developed to ease timing constraints, not obtain speed and power benefits
- NULL Convention Logic (NCL)
  - synthesis performed at gate level
    - 27 fundamental state-holding gates plus inverting and resettable variations
  - can use standard EDA tools with slight modification
- Seitz's method, Anantharaman's approach, DIMS, Singh's method and David's method
  - synthesis performed at gate level
    - only one type of state-holding gate: the C-element

# Commercial Asynchronous Endeavors

- Achronix (PCHB)
  - demonstrated 650+ MHz FPGA using 180 nm design rules
  - will introduce an Ultra line of FPGAs later this year
    - fabricated with 90 nm CMOS
    - operate at clock frequencies in the 700 MHz - 1.2 GHz range
    - based on a synchronous interface with asynchronous core
    - packaged with software tools to convert synchronous designs to asynchronous logic
- Fulcrum (PCHB)
  - targeting networking processing applications with asynchronous technology and EDA tools
  - PivotPoint SPI-4 switch chip, now used by about 15 vendors
    - 10 Gbit speed and 200 ns total latency through the chip
    - conservative, low-leakage 130 nm process
- Handshake Solutions (synchronous/asynchronous combination)
  - focused on low-power advantages of clockless logic, where it's successful in the smart-card market
    - sold millions of 8-bit asynchronous microcontrollers
  - working with Royal Philips Electronics and ARM Ltd. on a low-power, 32-bit processor designed for the auto market
- Silistix (GALS)
  - developing globally asynchronous, locally synchronous interconnect fabric and supporting EDA tools
- Theseus Logic (NCL)
  - low-power optimized asynchronous logic methodology based on commercial EDA tools
  - developing low-cost, highly integrated mixed-signal systems-on-chip for wireless sensor nodes
  - developed NCL implementation of Motorola HCS08 microprocessor
  - developed asynchronous FPGA based on Atmel AT40K family