

Quad-Rail Combinational Circuit Design Example Problems

- 1) Design a fully observable and input-complete quad-rail 2:1 multiplexer **having a worse-case delay of no more than two gates**. The inputs are $D0$ and $D1$, which are quad-rail signals, and S , which is a dual-rail signal; and the output is F , which is a quad-rail signal.

- 2) An unsigned NCL dual-rail pipelined Booth2 multiplier has a worse case combinational stage delay of 3 gates for the partial product (PP) generation when designed as a single combinational block, which limits the maximum attainable throughput for the entire pipeline. To increase the pipeline's throughput, the PP generation circuitry could be partitioned into two stages. Draw the maximum speed, minimal area logic diagram for the circuit to recode the PP selection bits, MR(2:0). The outputs are a dual-rail sign bit, S , which is logic 0 when the PP is positive and logic 1 when the PP is negative, and a quad-rail signal, sel , which follows the table given below. The circuit must be input-complete with respect to MR(2:1).

MR_2	MR_1	MR_0		PP		PP		sel
0	0	0		+0		+0		0
0	0	1		+MD		\pm MD		1
0	1	0		+MD		\pm 2MD		2
0	1	1		+2MD		-0		3
1	0	0		-2MD				
1	0	1		-MD				
1	1	0		-MD				
1	1	1		-0				