VHDL Design Project

Problem: Design a Generic NCL 2^s Complement MAC

* entity name: *MAC*
* generic constants: *X_len*, *Y_len*: positive, default to 4 (X_len ≤ Y_len); *A_len*: positive, default to 8
* inputs: *X*, *Y*: arbitrary length dual_rail_logic_vector (assume ≥ 4); *reset*, *Ki*: std_logic
* outputs: *A*: arbitrary length dual_rail_logic_vector (assume ≥ X_len+Y_len);
  OV: dual_rail_logic; *Ko*: std_logic

* name your file: MAC_group#.vhd
* include as comments: name and student number of group members (-- precedes a comment line)
* use the array structured multiplication algorithm

* email your main design, components, and testbench(es) as attachments from the PC (ftp to PC) to:
  insert email address here
* your design will then be run on my testbenches
* make sure that all names and input/output order match those on this sheet, otherwise your design will not run on my testbenches and points will be deducted

* Turn in a report including the following
  - Project Description
  - Block Diagram of MAC Chip
  - Gate-level Design of MAC Components (i.e. FA, HA, AND2, NAND2, FA1, HA1, OVcomp, etc.)
  - Component-level diagram of the following sized MACs
    > 8+4×4
    > 12+5×4
  - MAC VHDL code
  - VHDL testbench(es), testing 8+4×4 and 12+5×4 MACs

Hints:
- register the overflow and take both *OV* and *A* from the register output
- remember that at least 3 registers are required in a feedback loop to avoid deadlock
- the following constructs may be helpful:
  type twoD_array is array(3 downto 0, 3 downto 0) of dual_rail_logic;
  signal intermediate: twoD_array;
  intermediate(3, 0) <= D; -- D is defined as dual_rail_logic

VLSI Design Project #1

Problem: Design Static and Semi-Static NCL 24+8×8 Unsigned Quad-Rail MACs

* entity name: *MAC*
* inputs: *X*, *Y*: 4-signal quad_rail_logic_vector; *reset*, *Ki*: std_logic
* outputs: *A*: 12-signal quad_rail_logic_vector; *OV*: dual_rail_logic; *Ko*: std_logic

* name your VHDL file: MAC_project1.vhd
* include as comments: name and student number of group members (-- precedes a comment line)

* email your main design, components, and testbench as attachments from the PC (ftp to PC) to: insert email address here
* your design will then be run on my testbench
* make sure that all names and input/output order match those on this sheet, otherwise your design will not run on my testbench and points will be deducted

* Turn in a report including the following
  - project description
  - block diagram of MAC chip
  - component level diagram of MAC chip
  - gate-level design of MAC components (i.e. FA, HA, AND2, OVcomp, etc.)
  - MAC VHDL code
  - VHDL testbench
  - VHDL simulation
  - transistor-level designs of semi-static NCL gates used in design
  - physical-level designs of semi-static NCL gates used in design
  - completed layout of MAC chip
  - transistor-level simulation of MAC chip
  - physical-level simulation of MAC chip
  - compare the static and semi-static designs in terms of area, speed, and energy per operation

Hints:
- register the overflow and take both *OV* and *A* from the register output
- remember that at least 3 registers are required in a feedback loop to avoid deadlock

Procedure:
- first, design the circuit as a structural VHDL model to check functional correctness, using the provided NCL library, then implement the circuit in DA using the provided static NCL library
- next, implement the necessary semi-static NCL gates, in a different directory, then copy the DA circuit into this directory
- simulate both designs using your VHDL testbench, by following the steps provided in [1], which can be downloaded at http://www.ece.umr.edu/~smithsco/

[1] A. Singh and S. C. Smith, "Using a VHDL Testbench for Transistor-Level Simulation and Energy Calculation," *The 2005 International Conference on Computer Design*, pp. 115-121, June 2005.

VLSI Design Project #2

Problem: Design Static and Semi-Static Bit-Wise Pipelined NCL 8×8 Array-Structured 2^s Complement Dual-Rail Multipliers

* entity name: *MULT8x8*
* inputs: *X*, *Y*: 8-bit dual_rail_logic_vector; *reset*, *Ki*: std_logic
* outputs: *P*: 16-bit dual_rail_logic_vector; *Ko*: std_logic

* name your VHDL file: MULT8x8_project2.vhd
* include as comments: name and student number of group members (-- precedes a comment line)

* email your main design, components, and testbench as attachments from the PC (ftp to PC) to: insert email address here
* your design will then be run on my testbench
* make sure that all names and input/output order match those on this sheet, otherwise your design will not run on my testbench and points will be deducted

* Turn in a report including the following
  - project description
  - block diagram of multiplier chip
  - component level diagram of multiplier chip
  - gate-level design of multiplier components (i.e. FA, HA, AND2, NAND2, FA1, HA1, etc.)
  - multiplier VHDL code
  - VHDL testbench
  - VHDL simulation
  - transistor-level designs of semi-static NCL gates used in design
  - physical-level designs of semi-static NCL gates used in design
  - completed layout of multiplier chip
  - transistor-level simulation of multiplier chip
  - physical-level simulation of multiplier chip
  - compare the static and semi-static designs in terms of area, speed, and energy per operation

Procedure:
- first, design the circuit as a structural VHDL model to check functional correctness, using the provided NCL library, then implement the circuit in DA using the provided static NCL library
- next, implement the necessary semi-static NCL gates, in a different directory, then copy the DA circuit into this directory
- simulate both designs using your VHDL testbench, by following the steps provided in [1], which can be downloaded at http://www.ece.umr.edu/~smithsco/

[1] A. Singh and S. C. Smith, "Using a VHDL Testbench for Transistor-Level Simulation and Energy Calculation," *The 2005 International Conference on Computer Design*, pp. 115-121, June 2005.

VLSI Design Project #3

Problem: Design Static and Semi-Static Full-Word Pipelined NCL 8×8 Booth2 2^s Complement Dual-Rail Multipliers

* entity name: *MULT8x8*
* inputs: *X*, *Y*: 8-bit dual_rail_logic_vector; *reset*, *Ki*: std_logic
* outputs: *P*: 16-bit dual_rail_logic_vector; *Ko*: std_logic

* name your VHDL file: MULT8x8_project3.vhd
* include as comments: name and student number of group members (-- precedes a comment line)

* email your main design, components, and testbench as attachments from the PC (ftp to PC) to: insert email address here
* your design will then be run on my testbench
* make sure that all names and input/output order match those on this sheet, otherwise your design will not run on my testbench and points will be deducted

* Turn in a report including the following
  - project description
  - block diagram of multiplier chip
  - component level diagram of multiplier chip
  - gate-level design of multiplier components (i.e. FA, HA, various PP generation circuits, etc.)
  - multiplier VHDL code
  - VHDL testbench
  - VHDL simulation
  - transistor-level designs of semi-static NCL gates used in design
  - physical-level designs of semi-static NCL gates used in design
  - completed layout of multiplier chip
  - transistor-level simulation of multiplier chip
  - physical-level simulation of multiplier chip
  - compare the static and semi-static designs in terms of area, speed, and energy per operation

Procedure:
- first, design the circuit as a structural VHDL model to check functional correctness, using the provided NCL library, then implement the circuit in DA using the provided static NCL library
- next, implement the necessary semi-static NCL gates, in a different directory, then copy the DA circuit into this directory
- simulate both designs using your VHDL testbench, by following the steps provided in [1], which can be downloaded at http://www.ece.umr.edu/~smithsco/

[1] A. Singh and S. C. Smith, "Using a VHDL Testbench for Transistor-Level Simulation and Energy Calculation," *The 2005 International Conference on Computer Design*, pp. 115-121, June 2005.