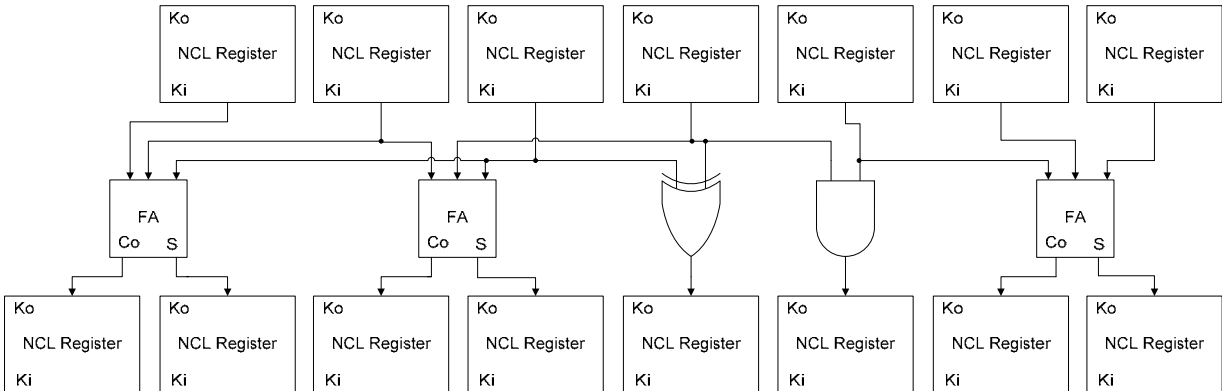
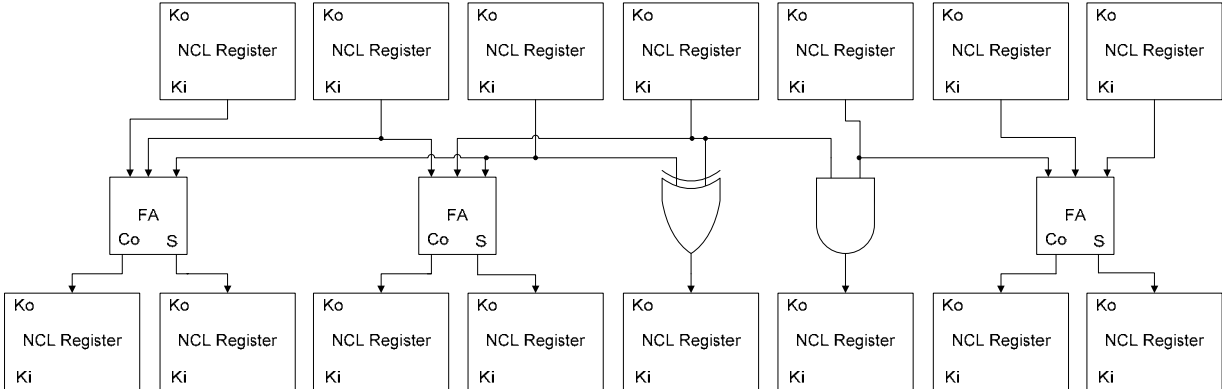


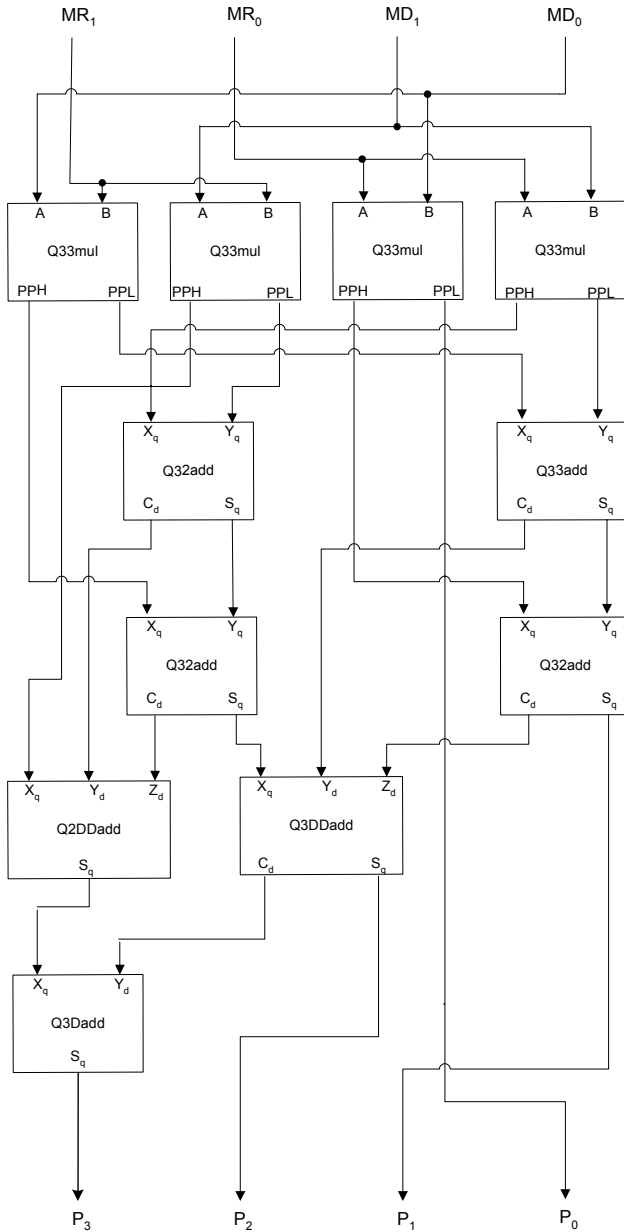
NCL Throughput Optimization Example Problems

1) For the following circuit, draw both the full-word and bit-wise completion components. Which completion strategy is better in terms of area? Which is better in terms of speed? Explain.



2) For the following quad-rail multiplier:

- i) Put an "X" through each component in the critical path(s). What is T_{DD} for the non-pipelined design?
- ii) If you were to maximize the throughput using full-word completion, what is the optimal T_{DD} and what is the minimal number of stages required? Show your work.
- iii) If you were to maximize the throughput using bit-wise completion, what is the optimal T_{DD} and what is the minimal number of stages required? Show your work.



Component Type	Output Gate Delays	
	Carry / PPH	Sum / PPL
Q33mul	1	2
Q33add	2	2
Q32add	2	2
Q3DDadd	2	2
Q2DDadd	N/A	2
Q3Dadd	N/A	1

- 3) The NULL Cycle Reduction (NCR) Technique for a dual-rail circuit is shown below. NCR can also be applied to quad-rail circuits by redesigning only the Demultiplexer and Multiplexer circuits.
- Redesign the NCR Multiplexer to handle quad-rail signals.
 - Redesign the NCR Demultiplexer to handle quad-rail signals.

