

Ultra-Low Power Applications

- Mobile computing
- Implantable medical device
- Remote sensor
- Space vehicle
- ...

Three Components of Power

- $P = C_L V_{DD}^2 f_{0 \rightarrow 1} + t_{sc} V_{DD} I_{peak} f_{0 \rightarrow 1} + V_{DD} I_{leakage}$

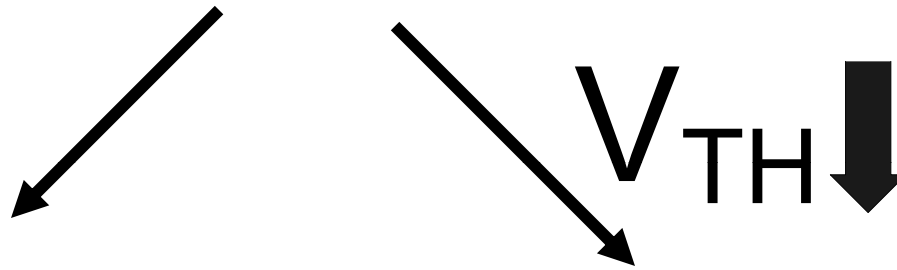
Dynamic
power

Short-circuit
power

Leakage
power

- $f_{0 \rightarrow 1} = Pro_{0 \rightarrow 1} * f_{clock}$

P ↓ ← **V_{DD}** ↓ $P \propto C_L V_{DD}^2$



T ↑

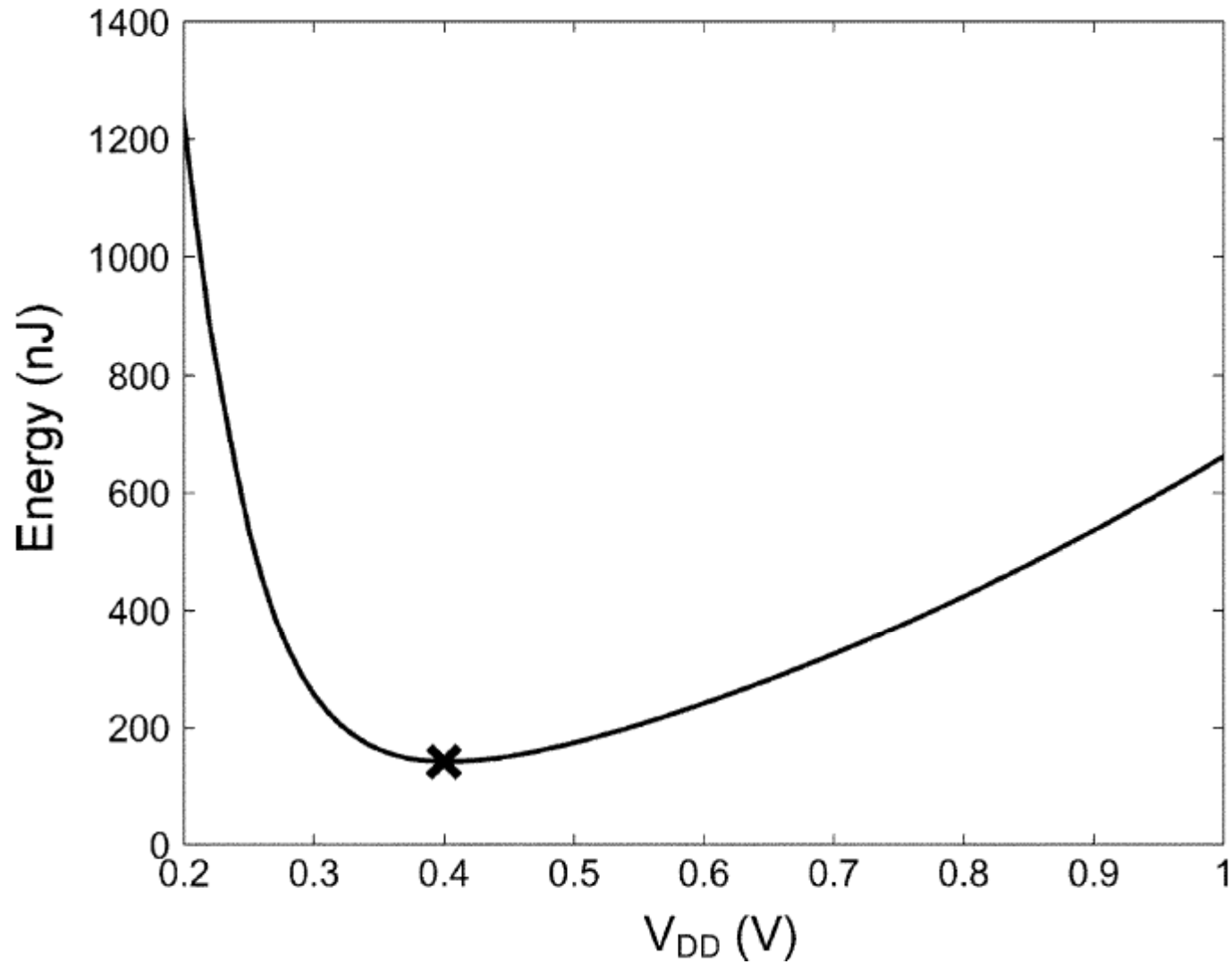
$$T \propto \frac{V_{DD}}{(V_{DD} - V_{th})^\alpha}$$

T ~

P_{LEAK} ↑

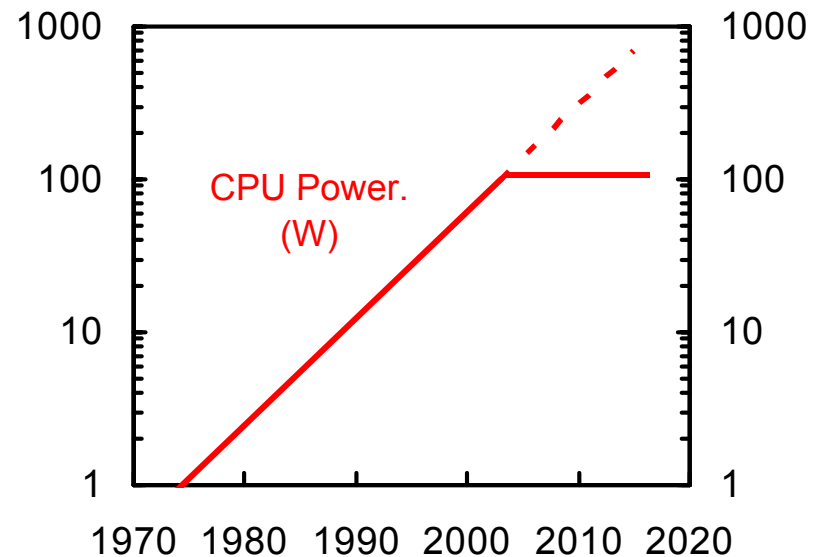
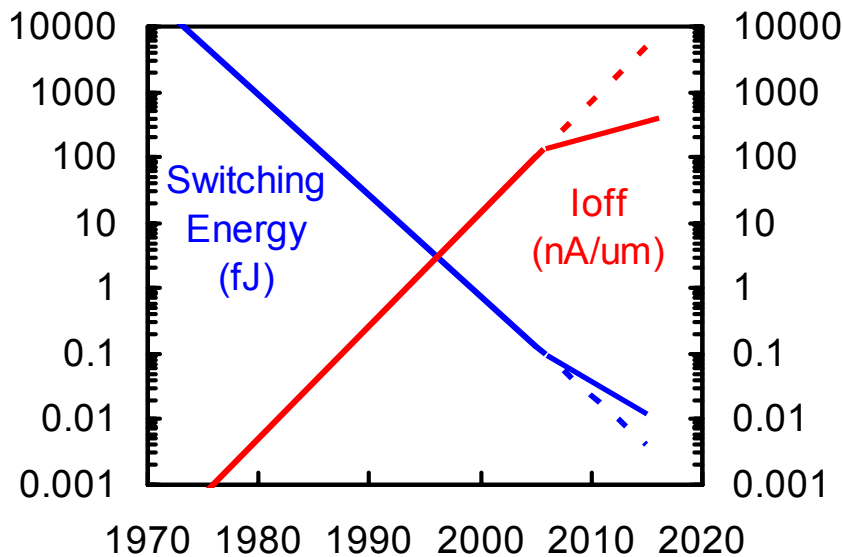
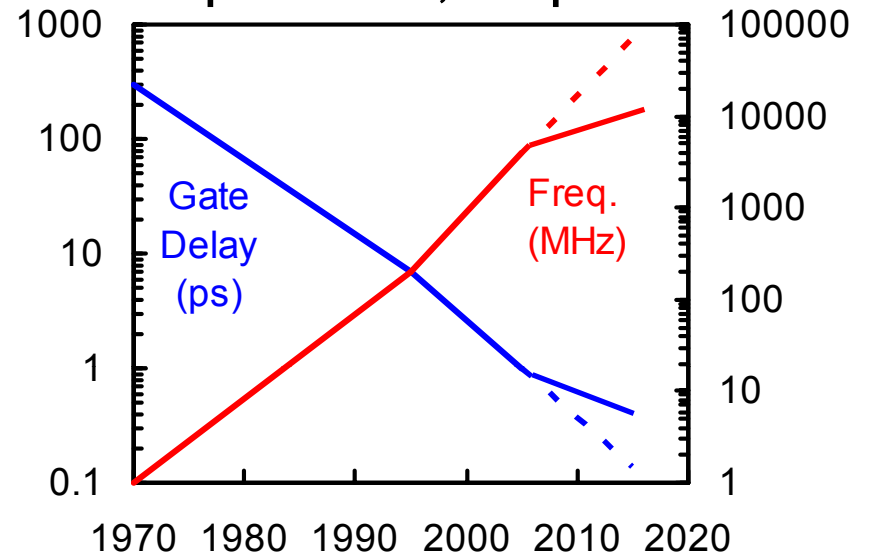
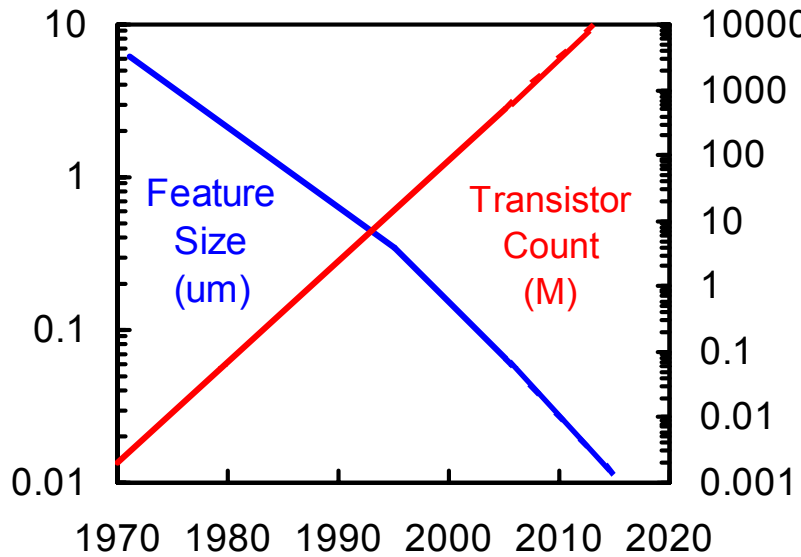
$$I_{leak} \propto e^{-\frac{V_{th}}{K}}$$

Sample Trend



Future Scaling- Foil courtesy Mark T. Bohr, Intel Senior

Fellow from his webcast at Intel Corporation, Sep 2006



Solution

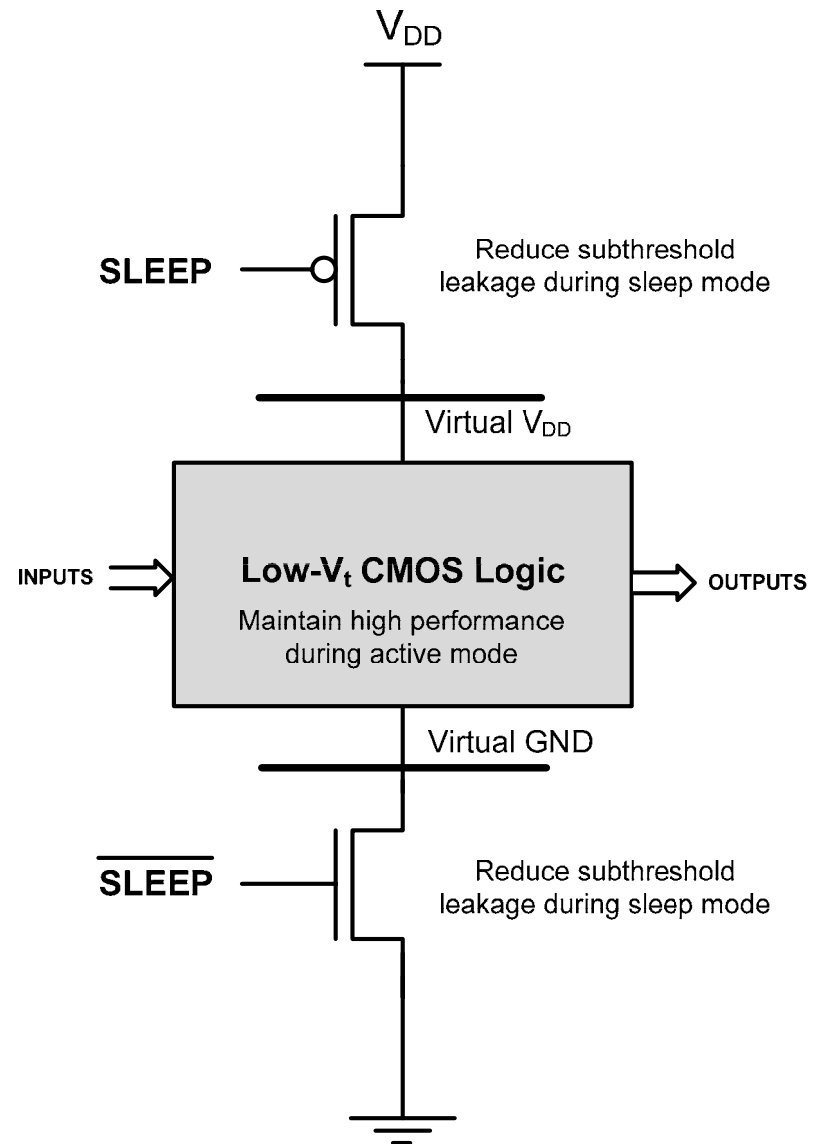
- Keep leakage under control while reducing V_{DD} and V_{TH}

Existing Methods

- Multi-Threshold CMOS (MTCMOS)
- Variable Threshold CMOS (VTCMOS)
- Dynamic Threshold MOS (DTMOS)
- Super Cut-off CMOS (SCCMOS)
- Forced Transistor Stacking
- Adaptive Body Bias (ABB)
- ...

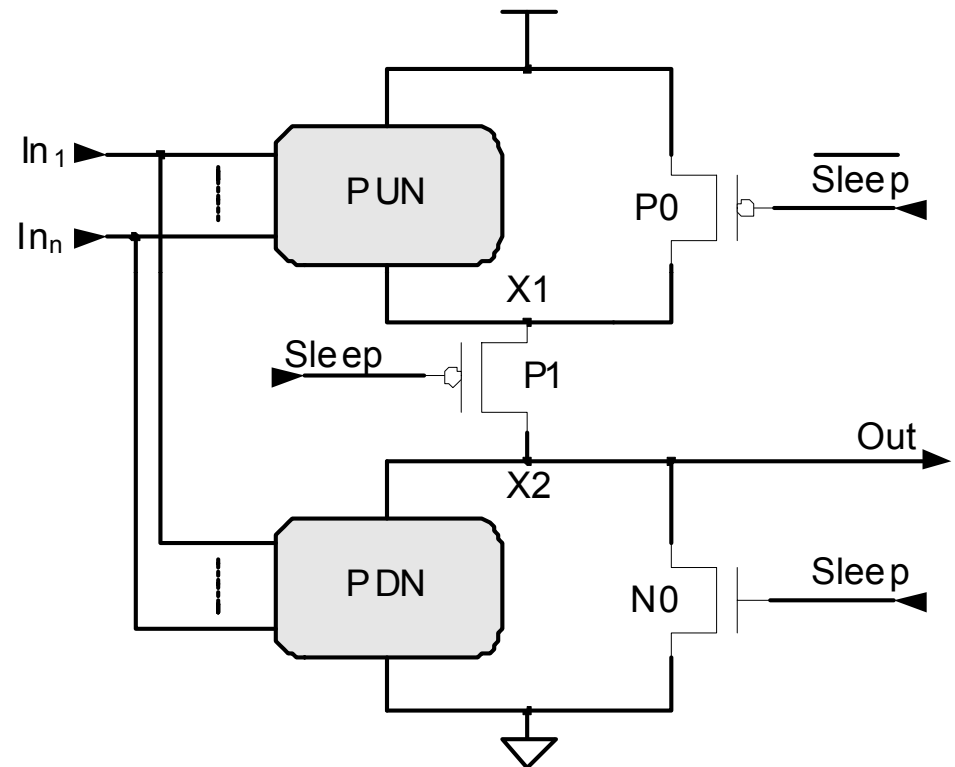
MTCMOS

- Utilize transistors with more than one V_{TH}
- Reduce leakage in “sleep” mode



Three Problems of MTCMOS Synchronous Circuits

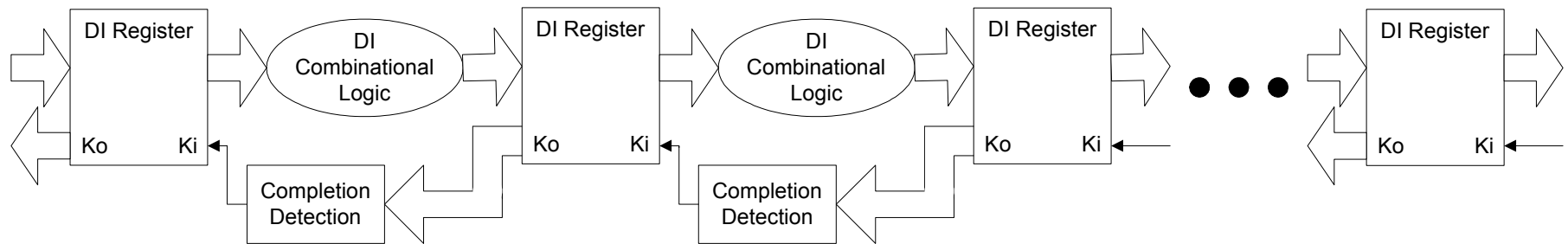
- *Sleep* signal generation
- Storage element data loss during sleep mode
- Sleep transistor sizing



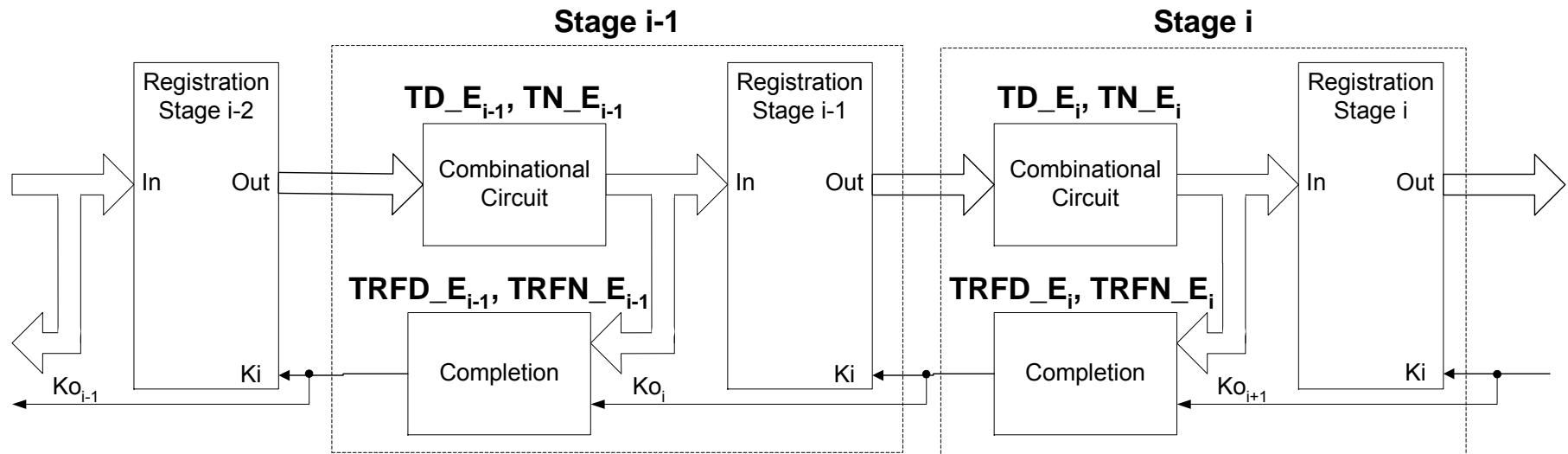
What will change if applying MTCMOS technique to NCL circuits?

Sleep Signal Generation and Data Storage for MTCMOS NCL Circuits

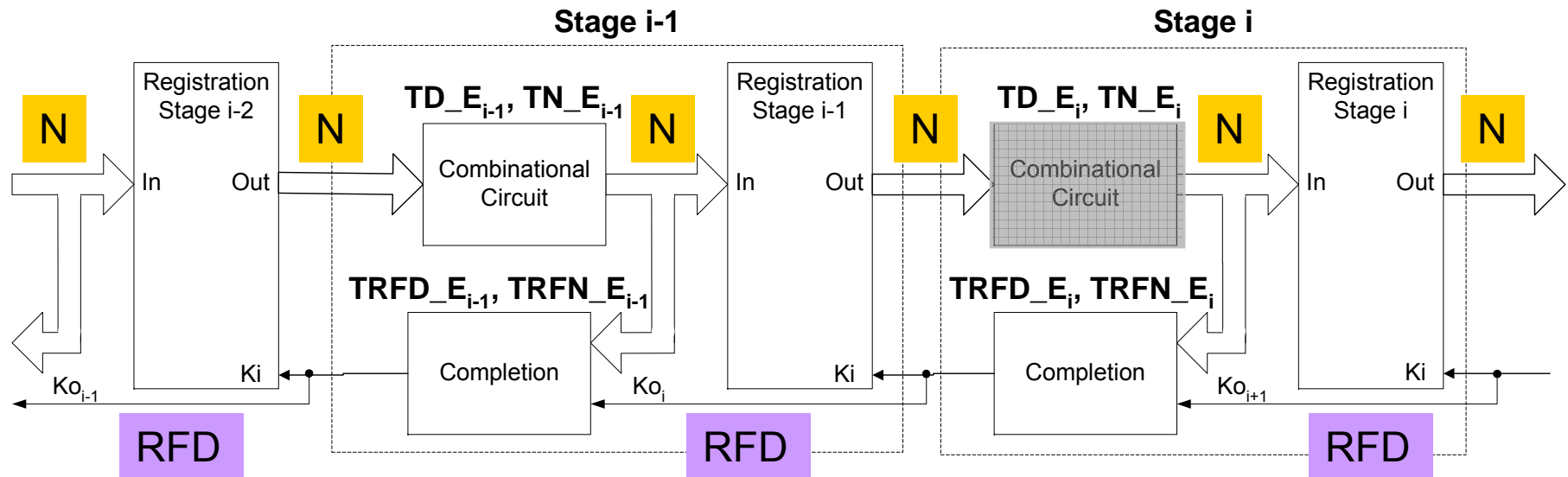
- The *Ko* signals naturally serve as inverted *Sleep* signals without any additional circuitry



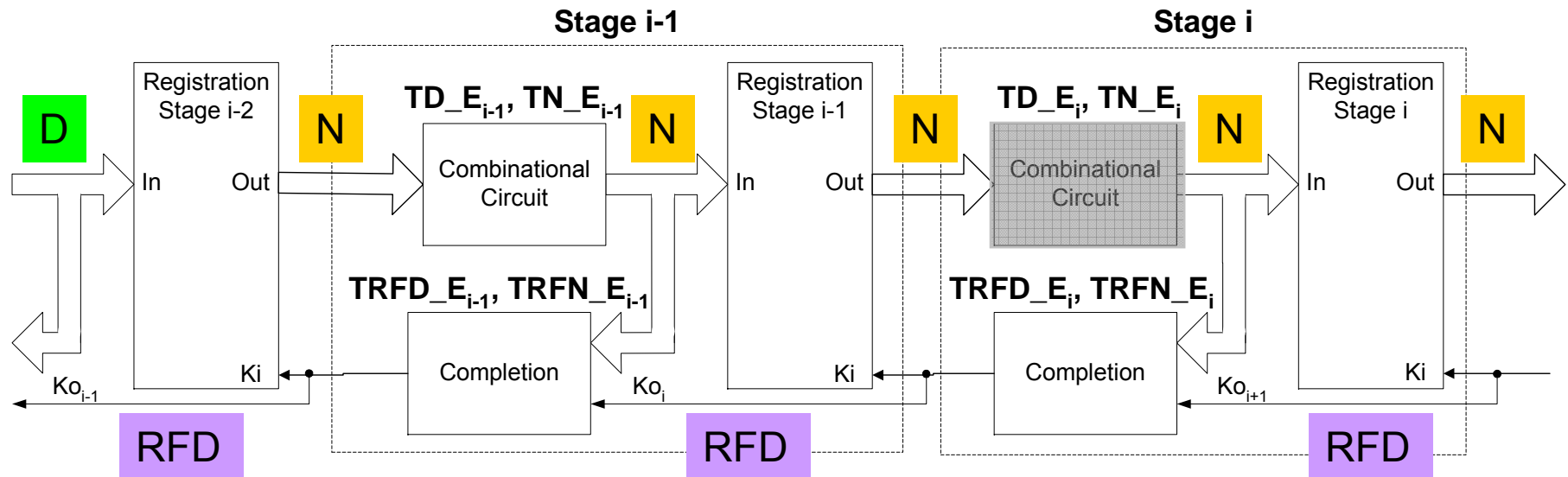
Use Early-Completion for Delay-Insensitivity



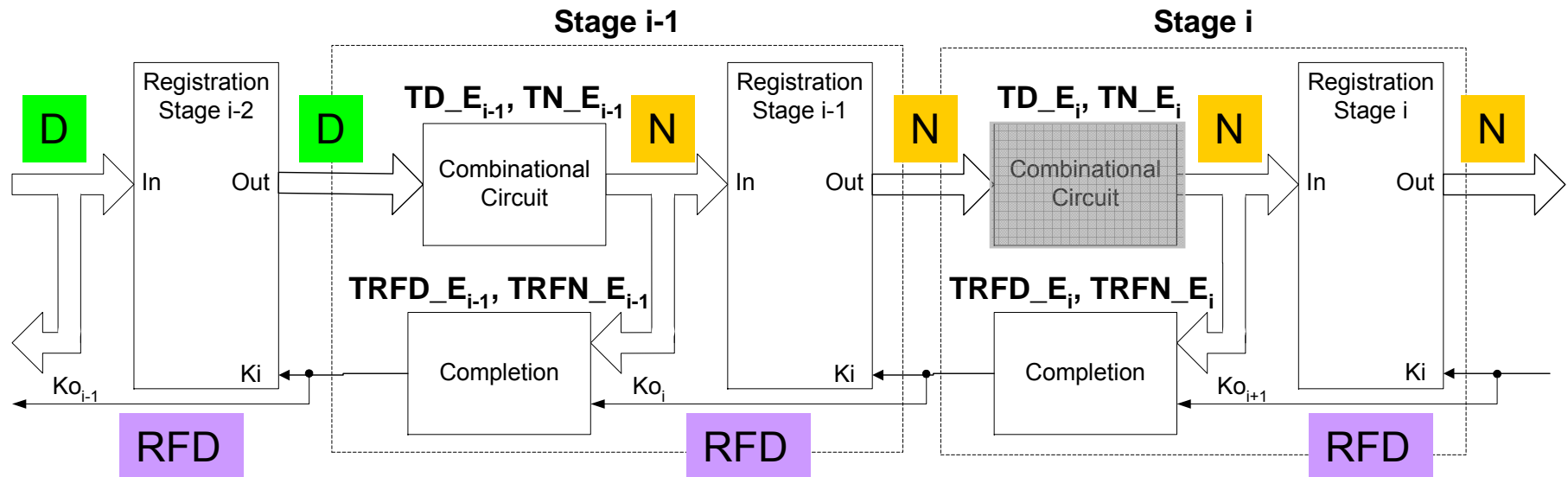
Use Early-Completion for Delay-Insensitivity (Cont')



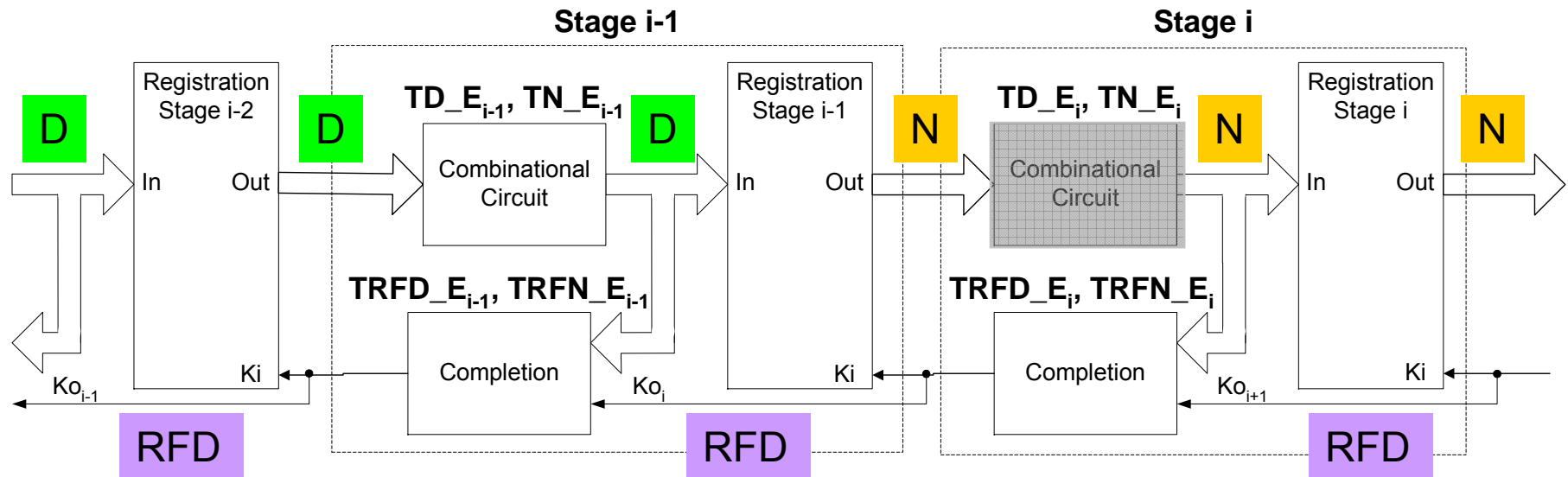
Use Early-Completion for Delay-Insensitivity (Cont')



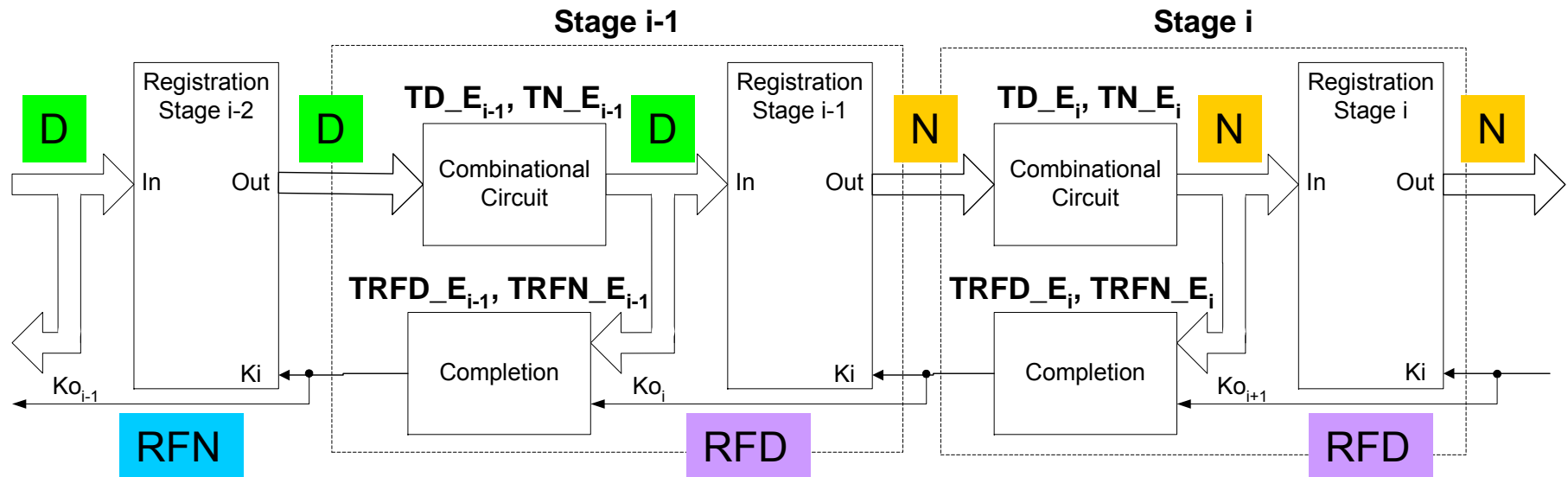
Use Early-Completion for Delay-Insensitivity (Cont')



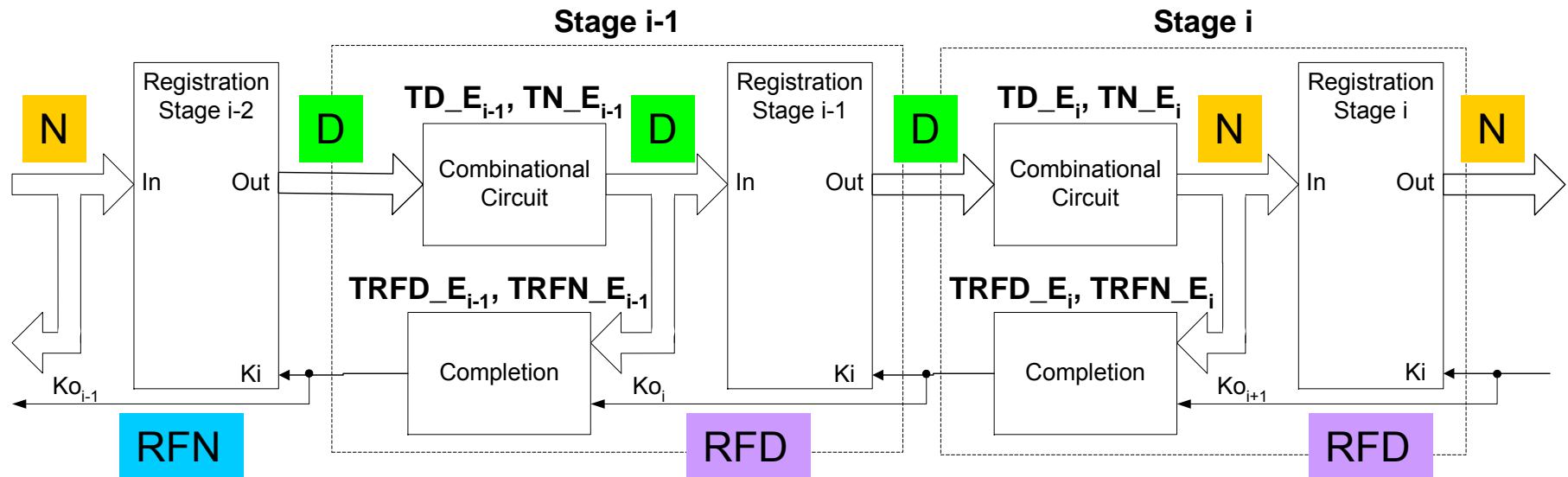
Use Early-Completion for Delay-Insensitivity (Cont')



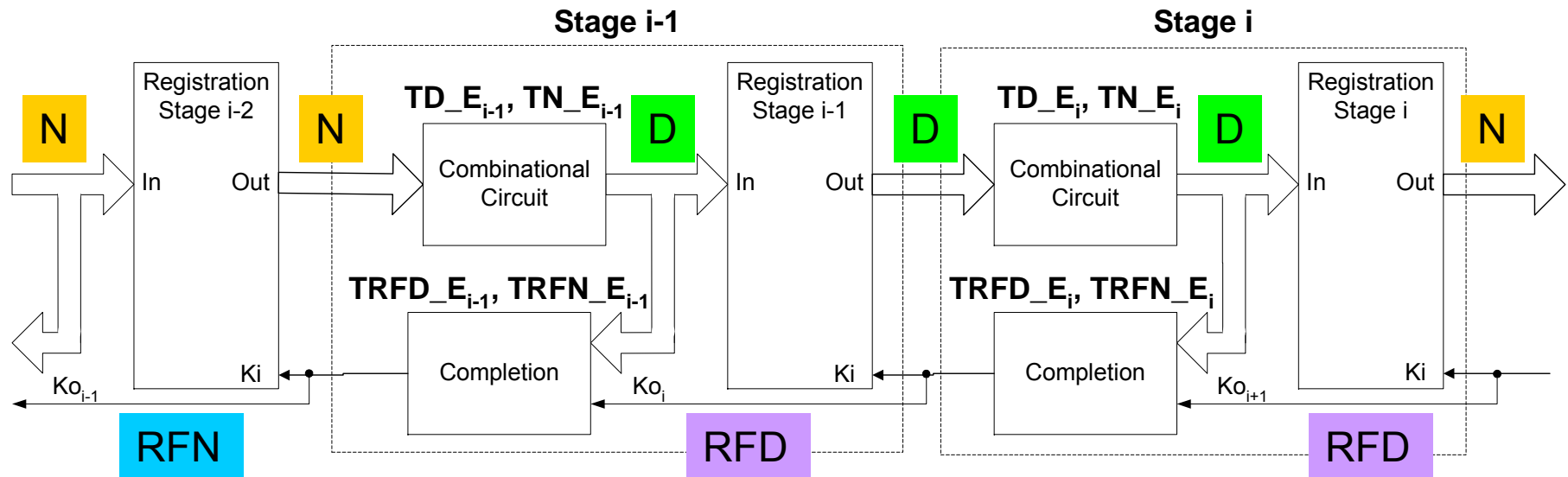
Use Early-Completion for Delay-Insensitivity (Cont')



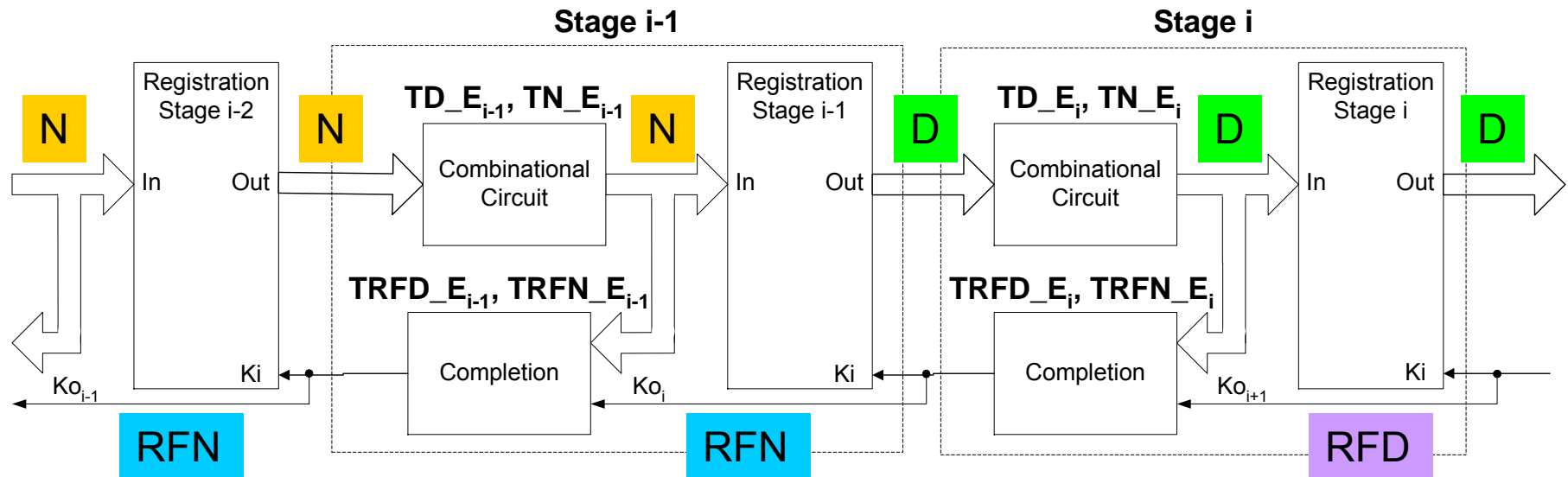
Use Early-Completion for Delay-Insensitivity (Cont')



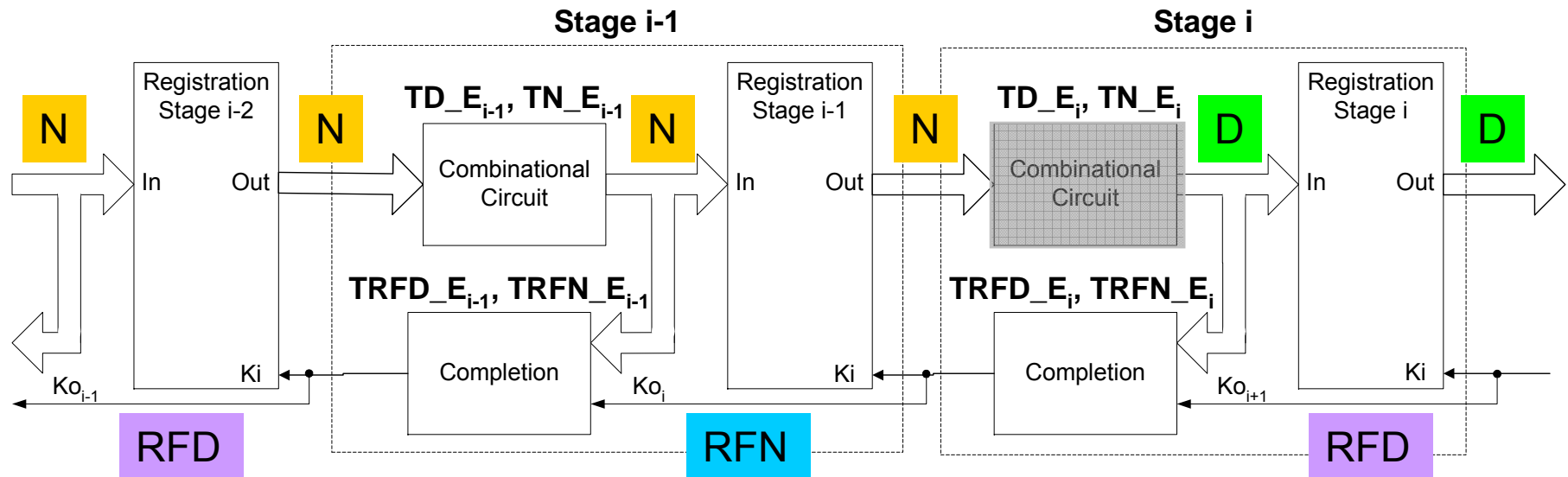
Use Early-Completion for Delay-Insensitivity (Cont')



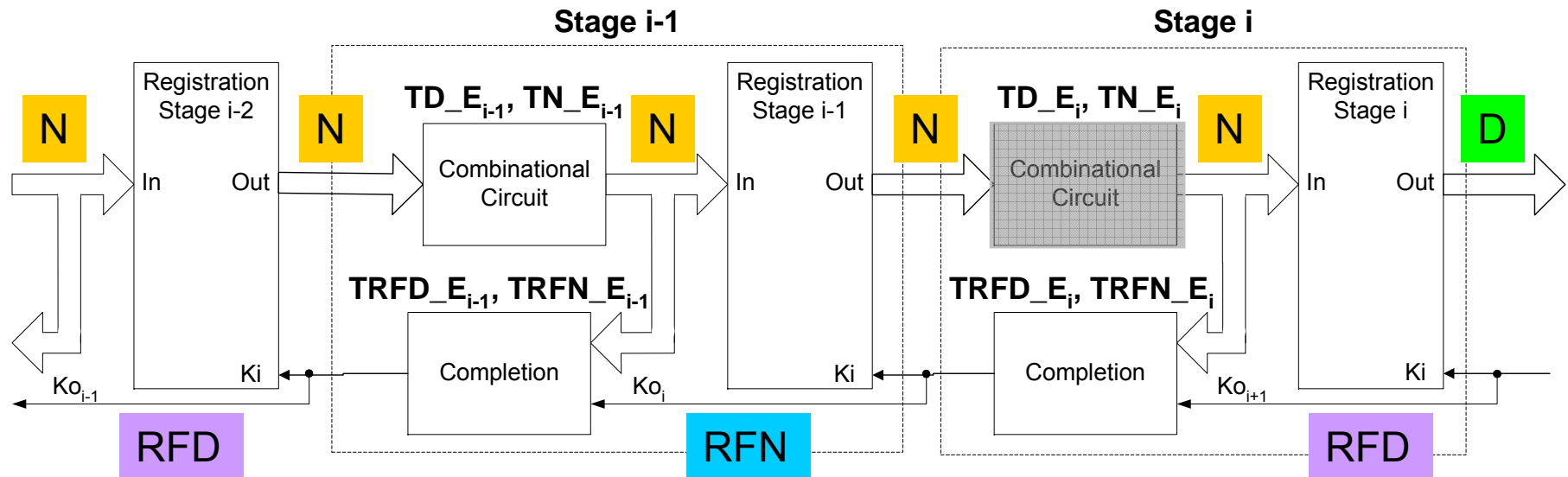
Use Early-Completion for Delay-Insensitivity (Cont')



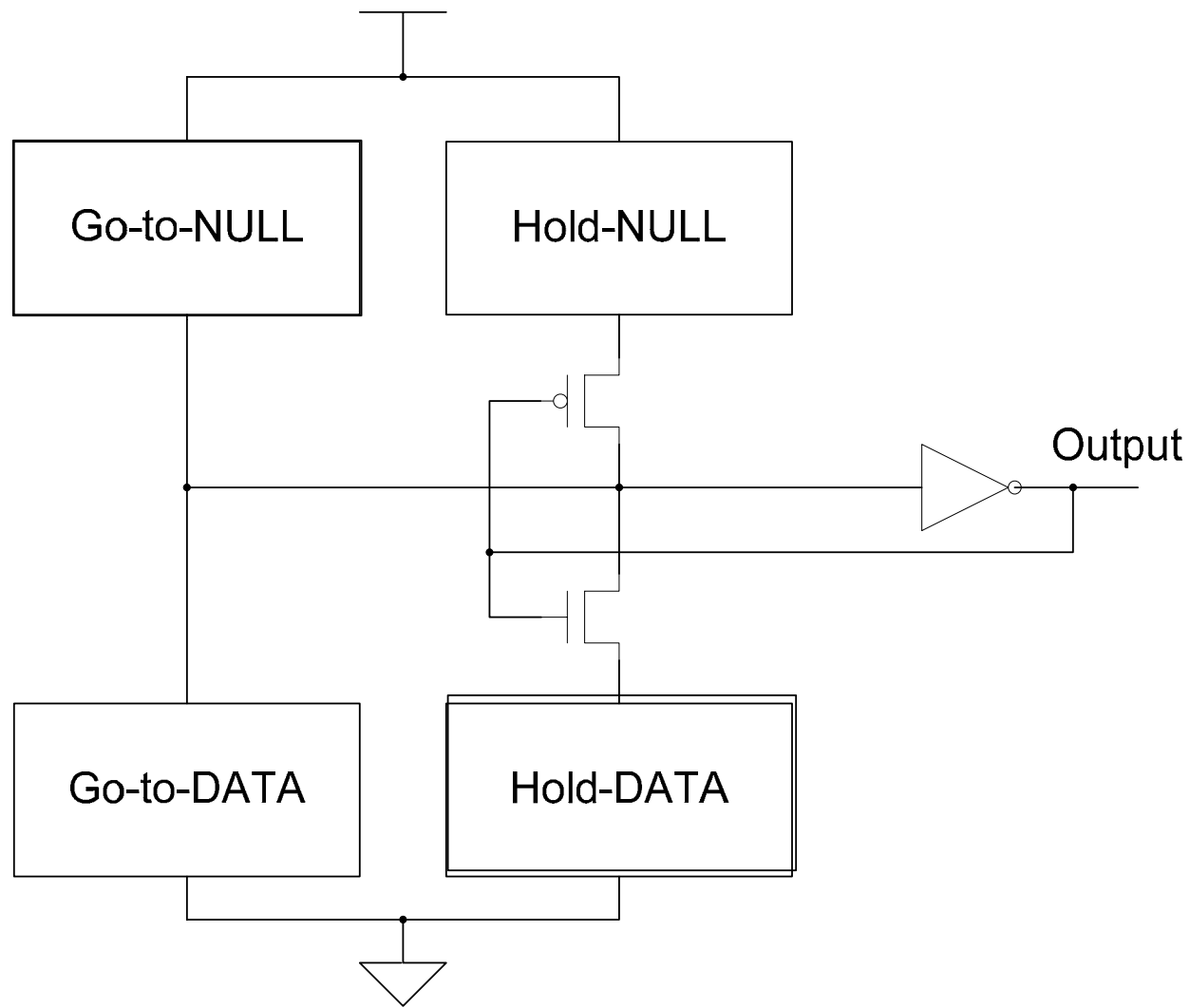
Use Early-Completion for Delay-Insensitivity (Cont')



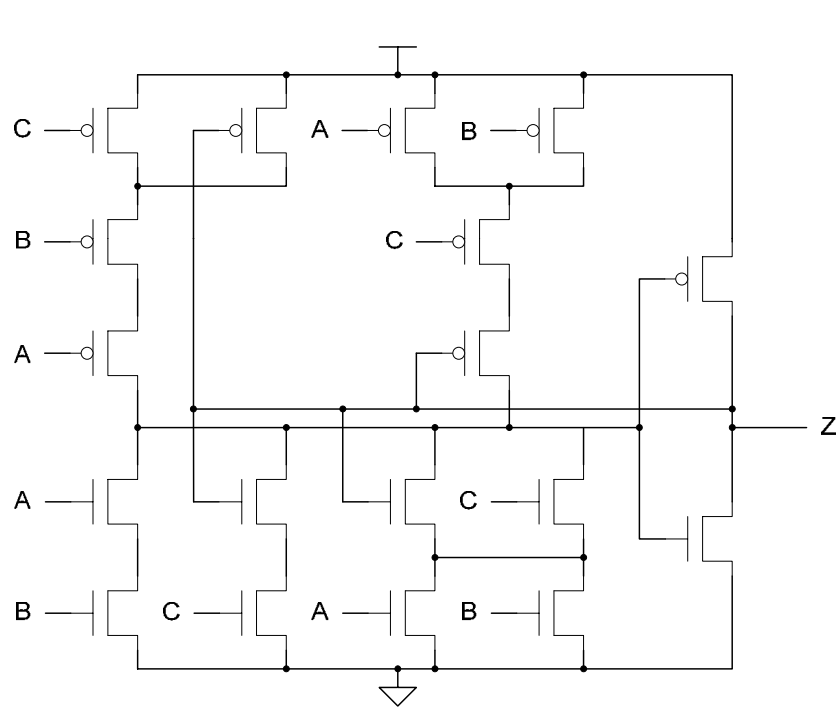
Use Early-Completion for Delay-Insensitivity (Cont')



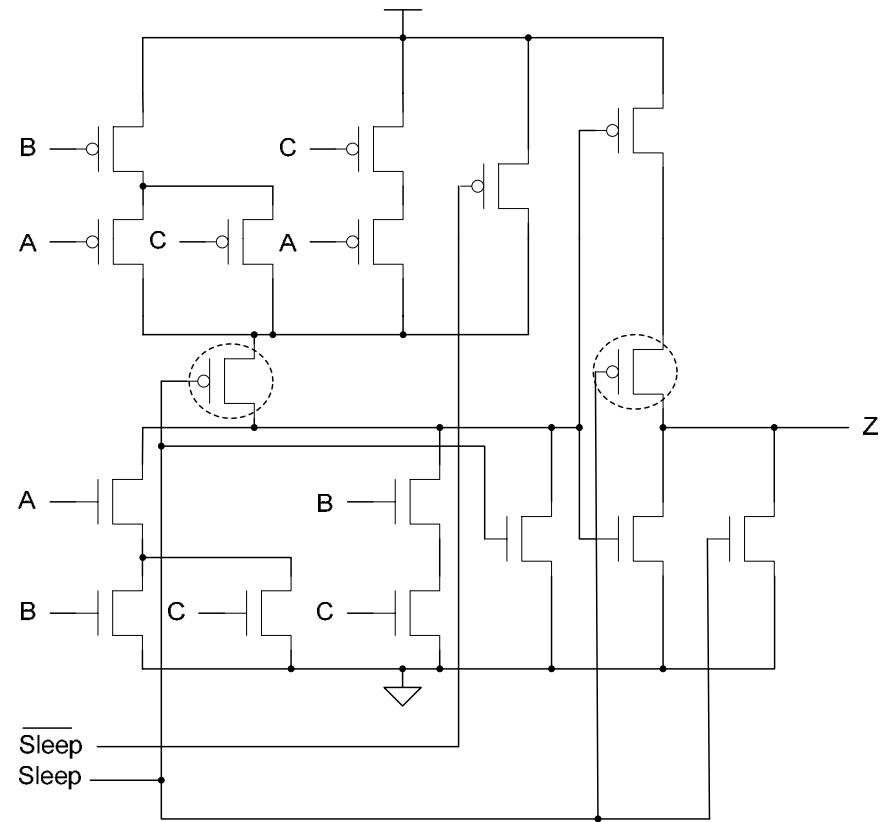
MTCMOS Threshold Gates



Sample TH23 Gates: Ease Sleep Transistor Sizing

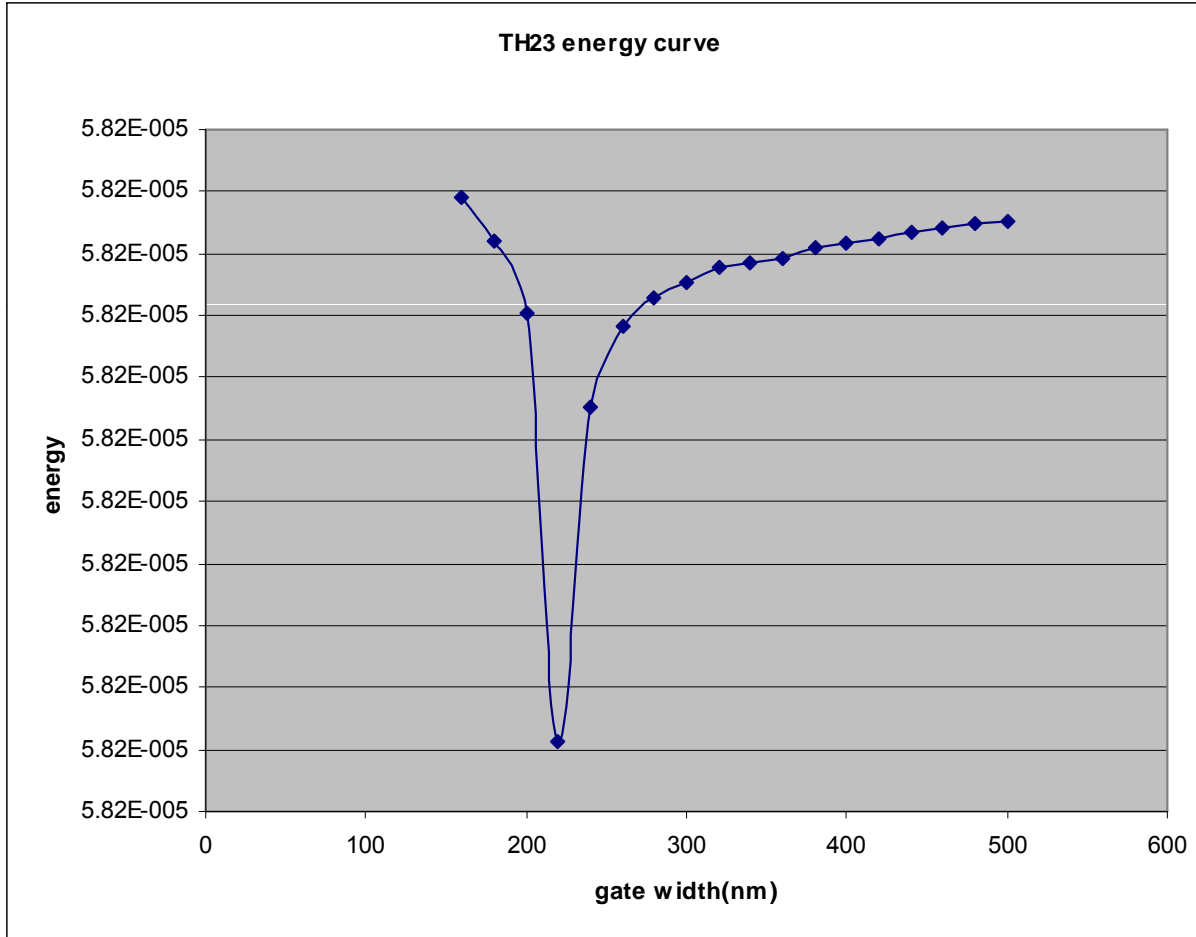


(a)



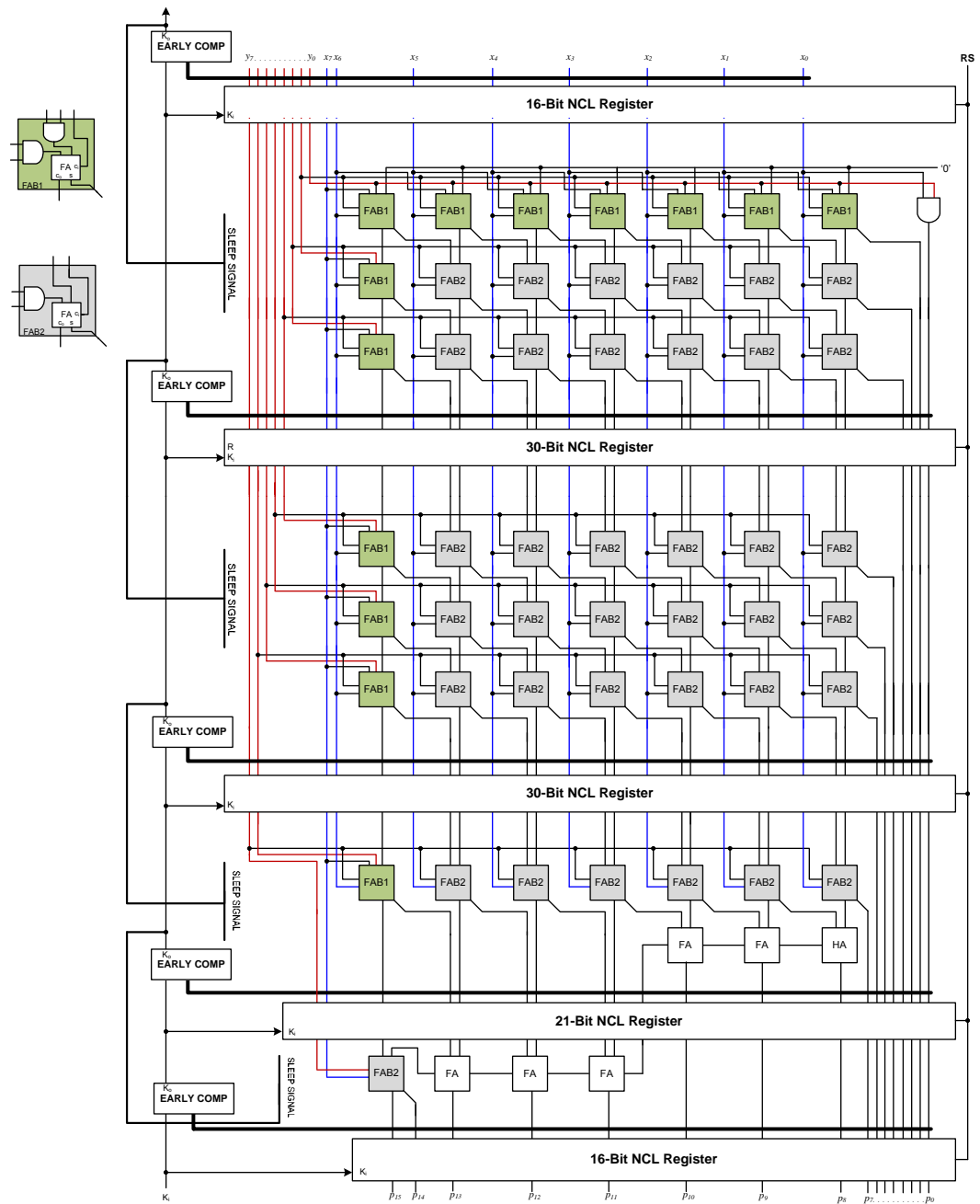
(b)

Sleep Transistor Sizing for TH23

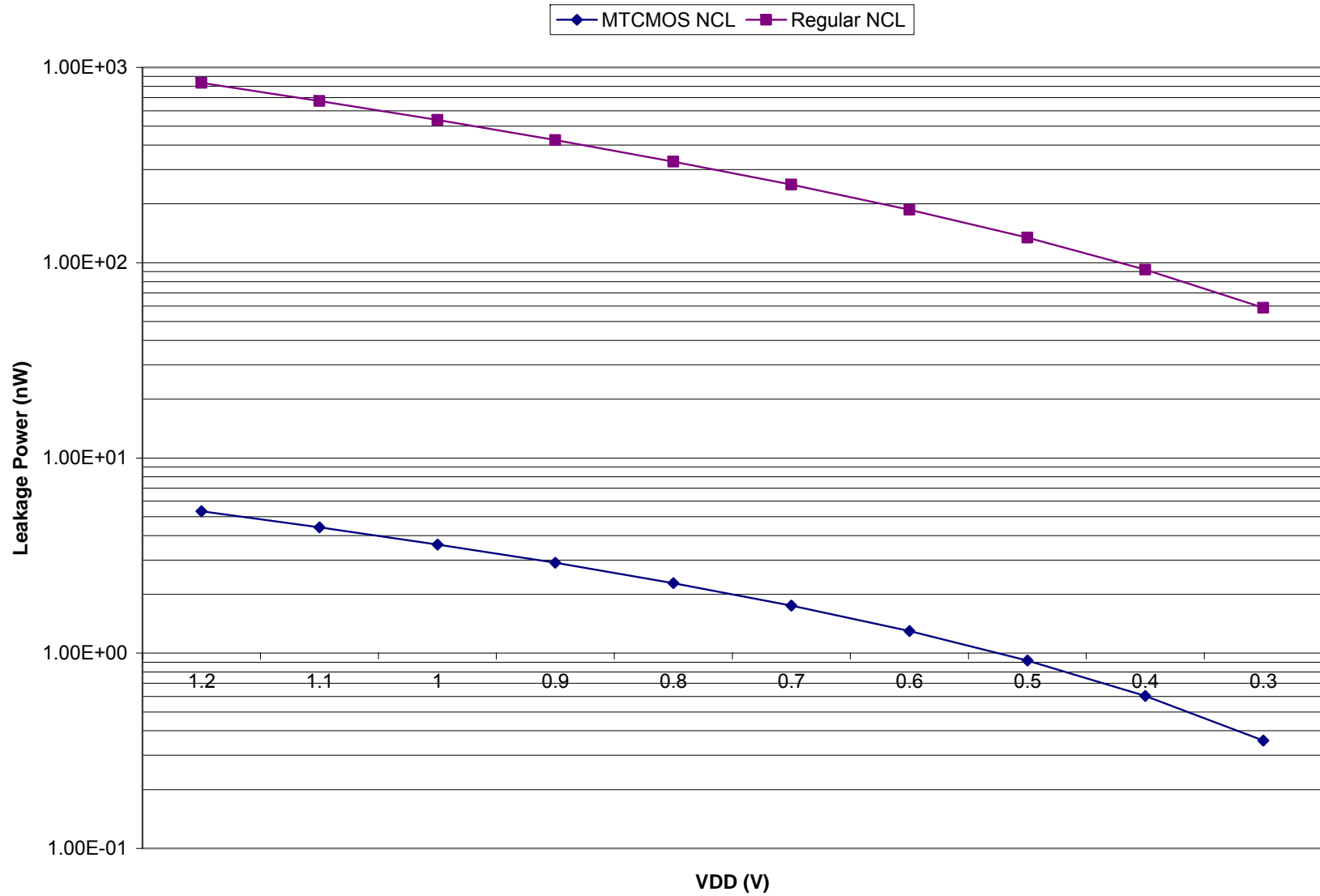


A 4-stage 8x8 MTCMOS NCL Unsigned Array Multiplier

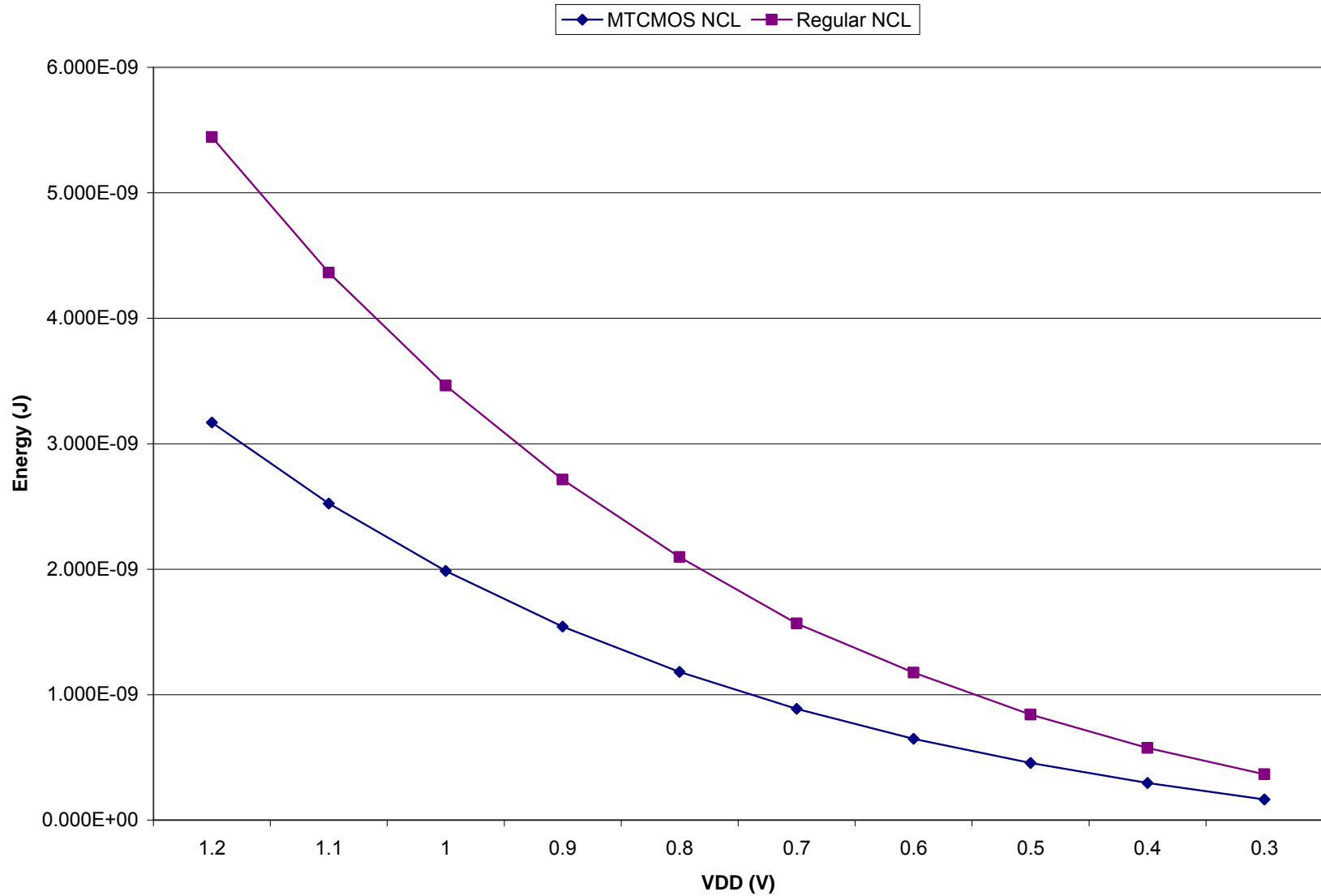
IBM 8RF-DM
0.13 μ m CMOS



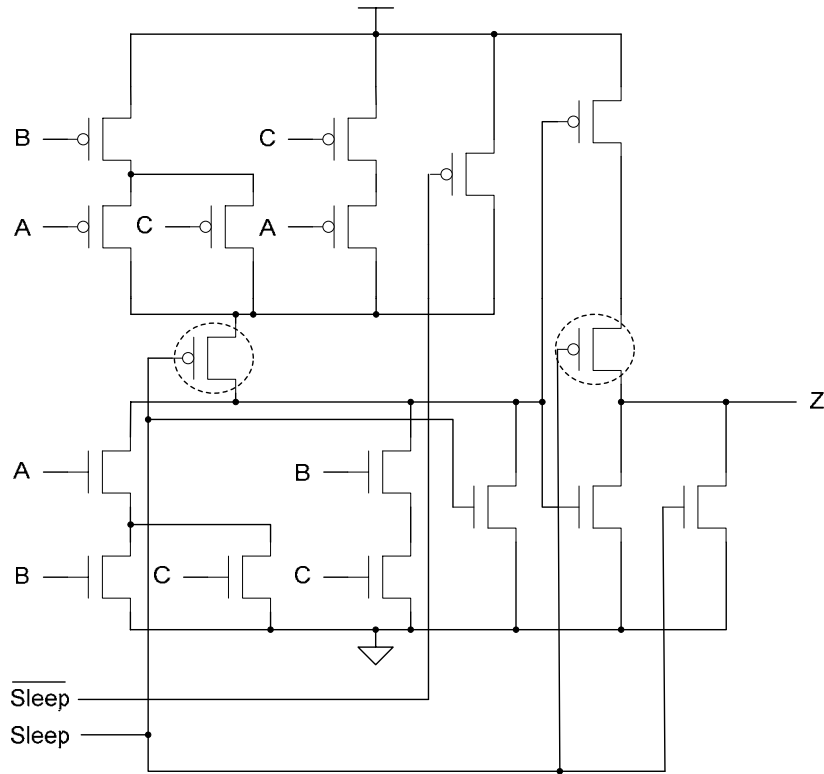
Leakage Power Comparison



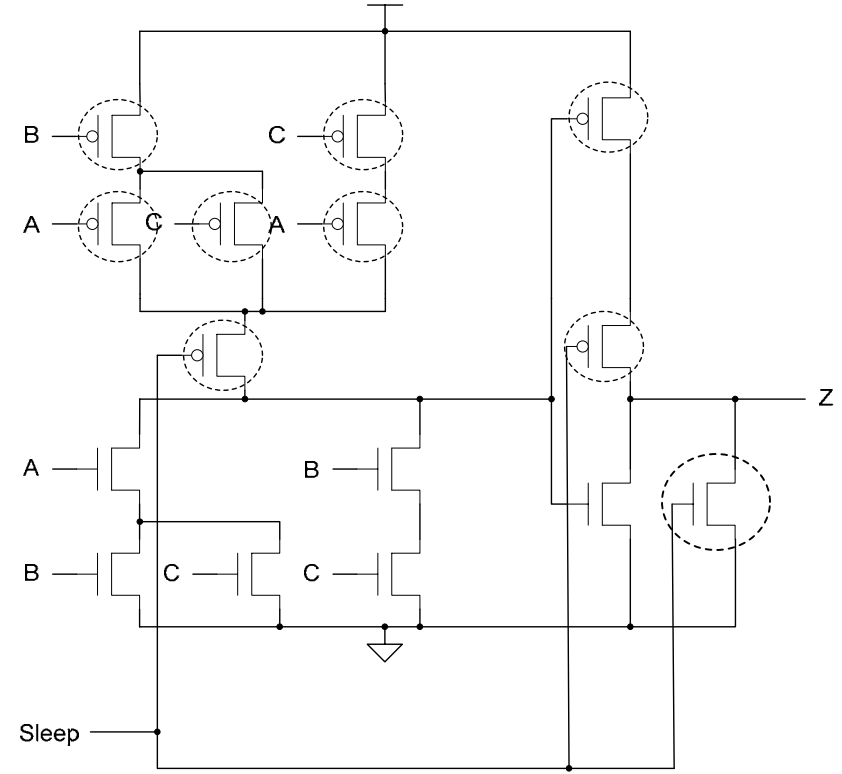
Active Energy Comparison



Further Improvement

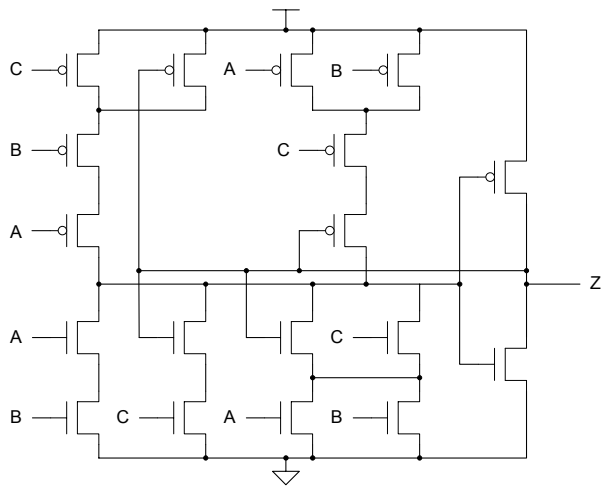


(b)

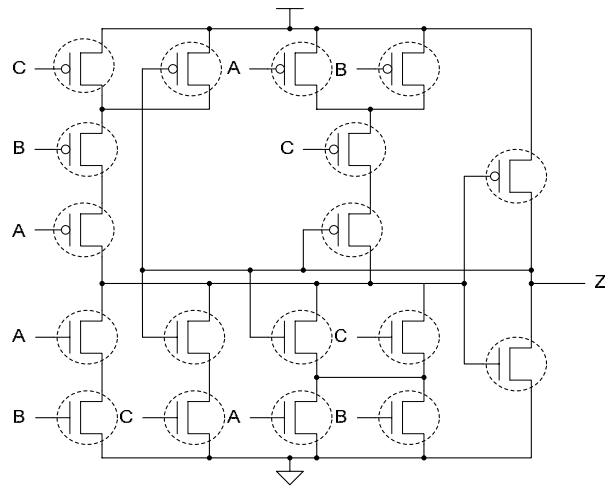


(c)

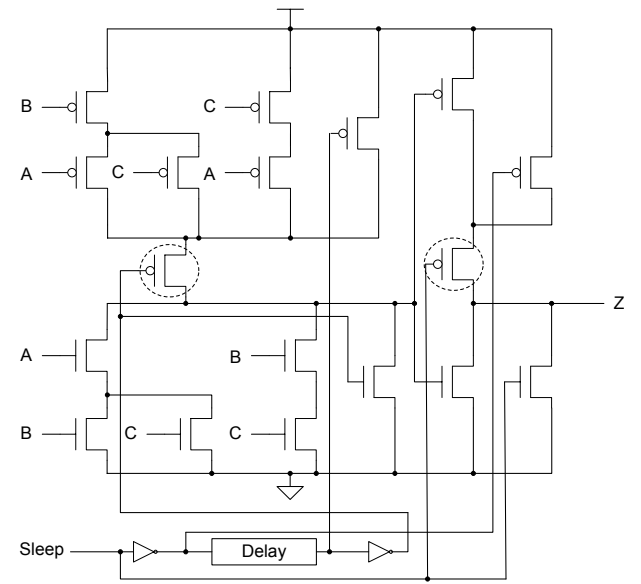
	Active Energy	Leakage Power	Delay 0→1	Delay 1→0
High V_T	6.84995	3.42488	1.32049	5.64464
Low V_T	6.85005	3.42491	1.27769	1.77329



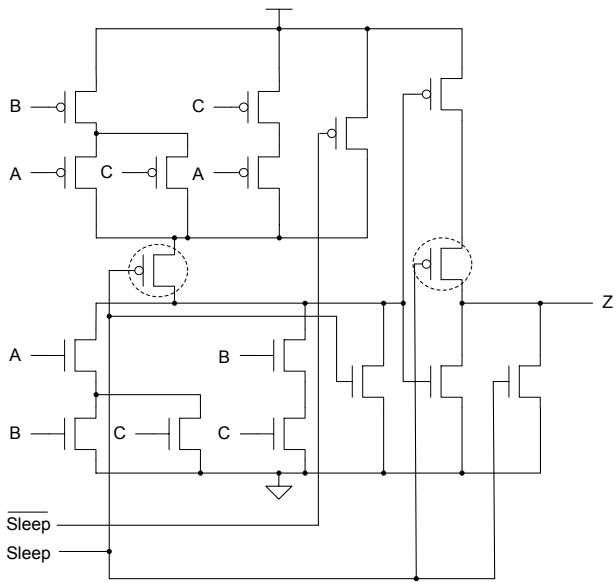
(RL)



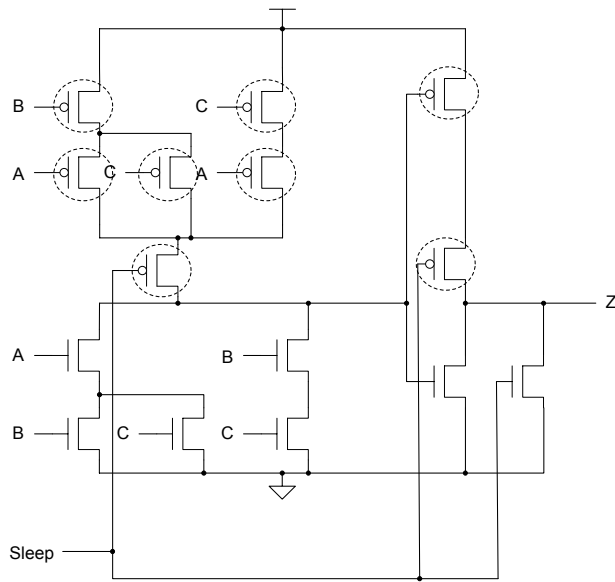
(RH)



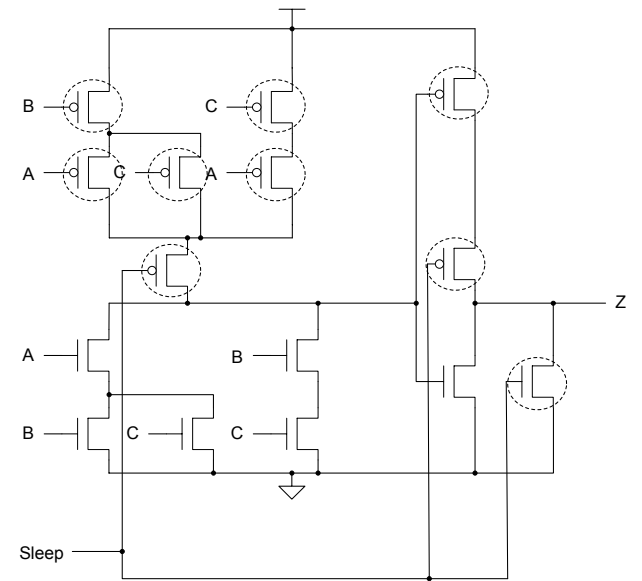
(INV)



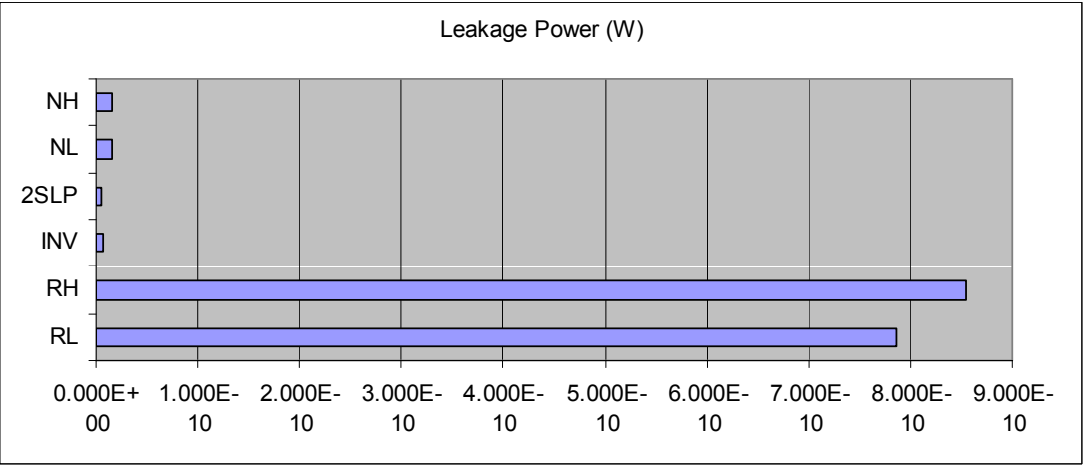
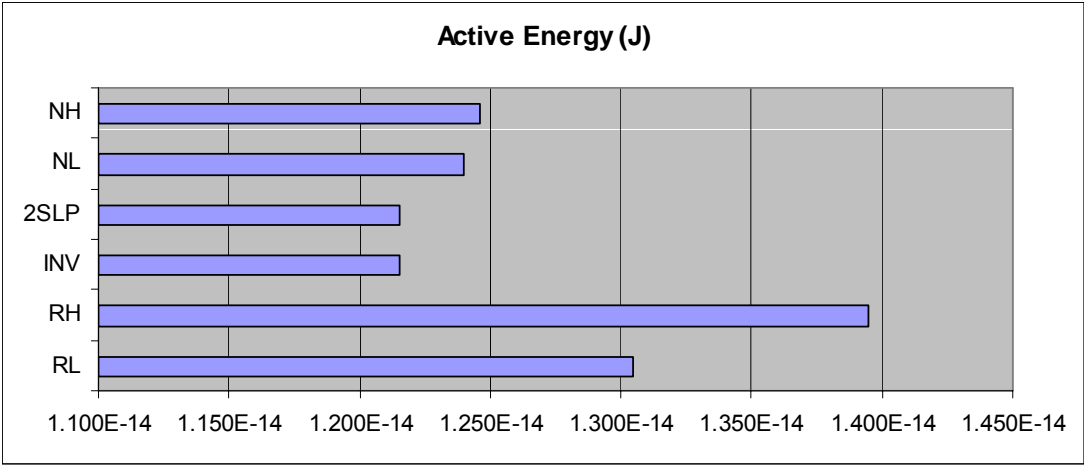
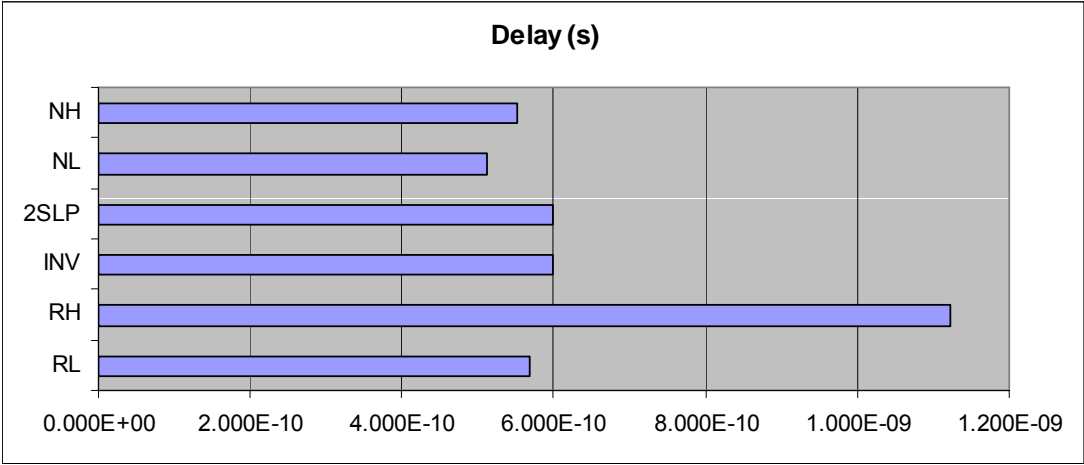
(2SLP)



(NL)



(NH)



Multiplier Comparison

- Six single-stage early-completion multipliers
- Six single-stage regular-completion multipliers
- Delay
- Active energy
- Leakage power

Early-Completion

