

NULL Convention Logic (NCL) Paradigm

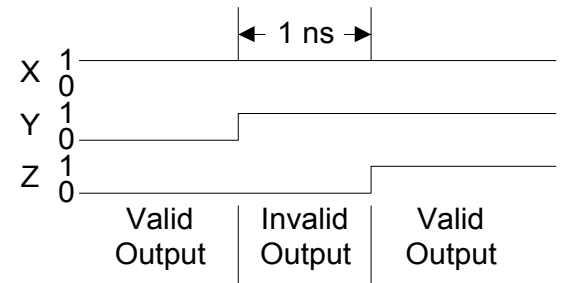
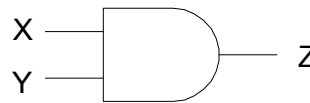
- Symbolically Complete
 - output value unambiguously specified irregardless of time reference

• Dual-Rail Encoding

	DATA0	DATA1	NULL	Illegal
Rail ⁰	1	0	0	1
Rail ¹	0	1	0	1

Boolean AND Gate

Symbolically Incomplete:
time reference required
for output validity

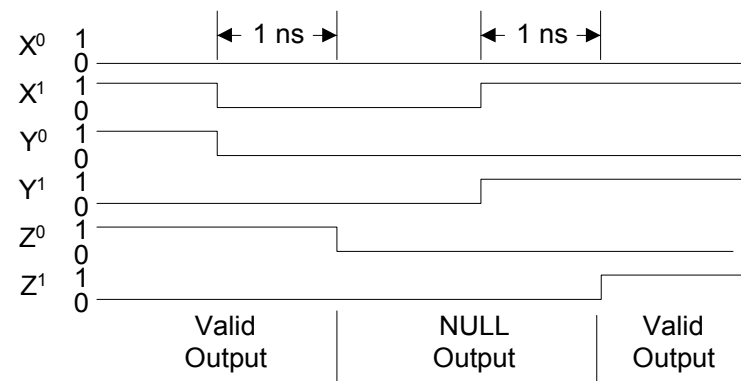
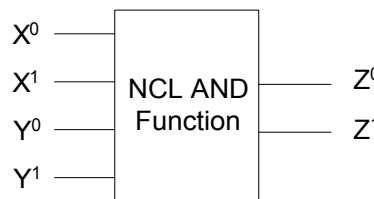


Quad-Rail Encoding

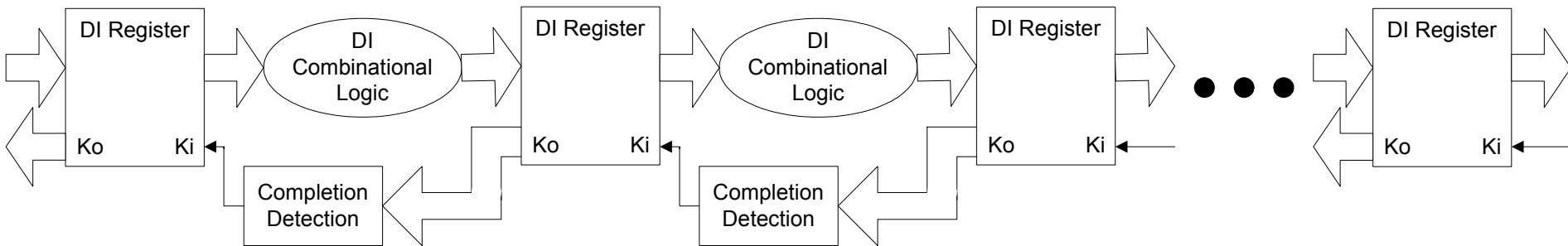
	DATA0	DATA1	DATA2	DATA3	NULL
Rail ⁰	1	0	0	0	0
Rail ¹	0	1	0	0	0
Rail ²	0	0	1	0	0
Rail ³	0	0	0	1	0

NCL AND Function

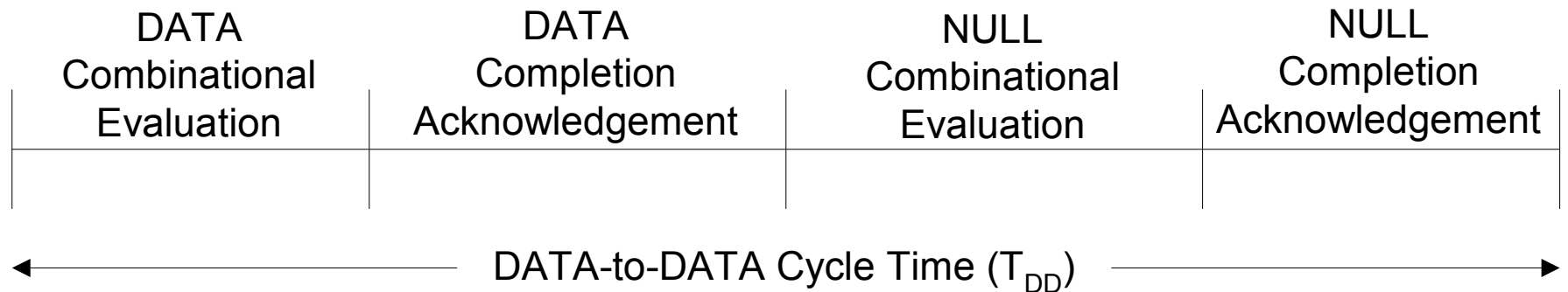
Symbolically Complete:
time not referenced,
output valid when
DATA (non-NULL)



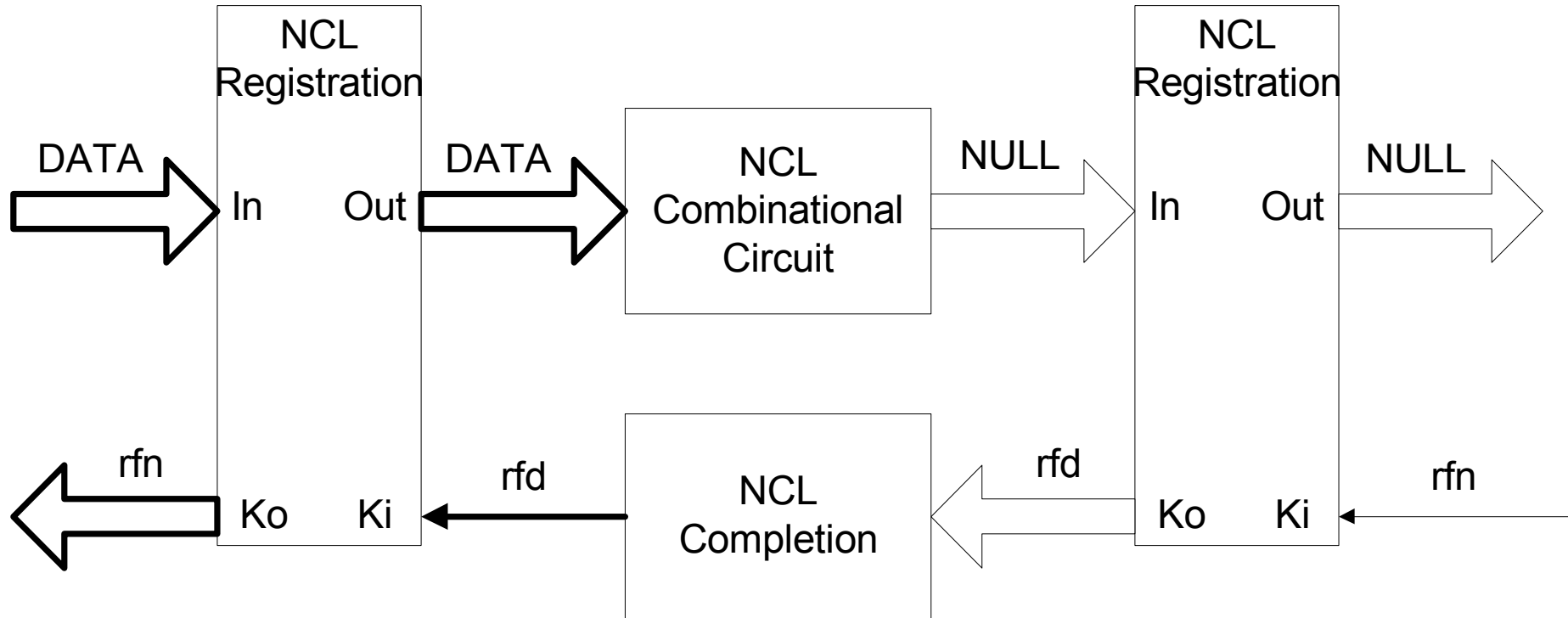
NCL Functional Components



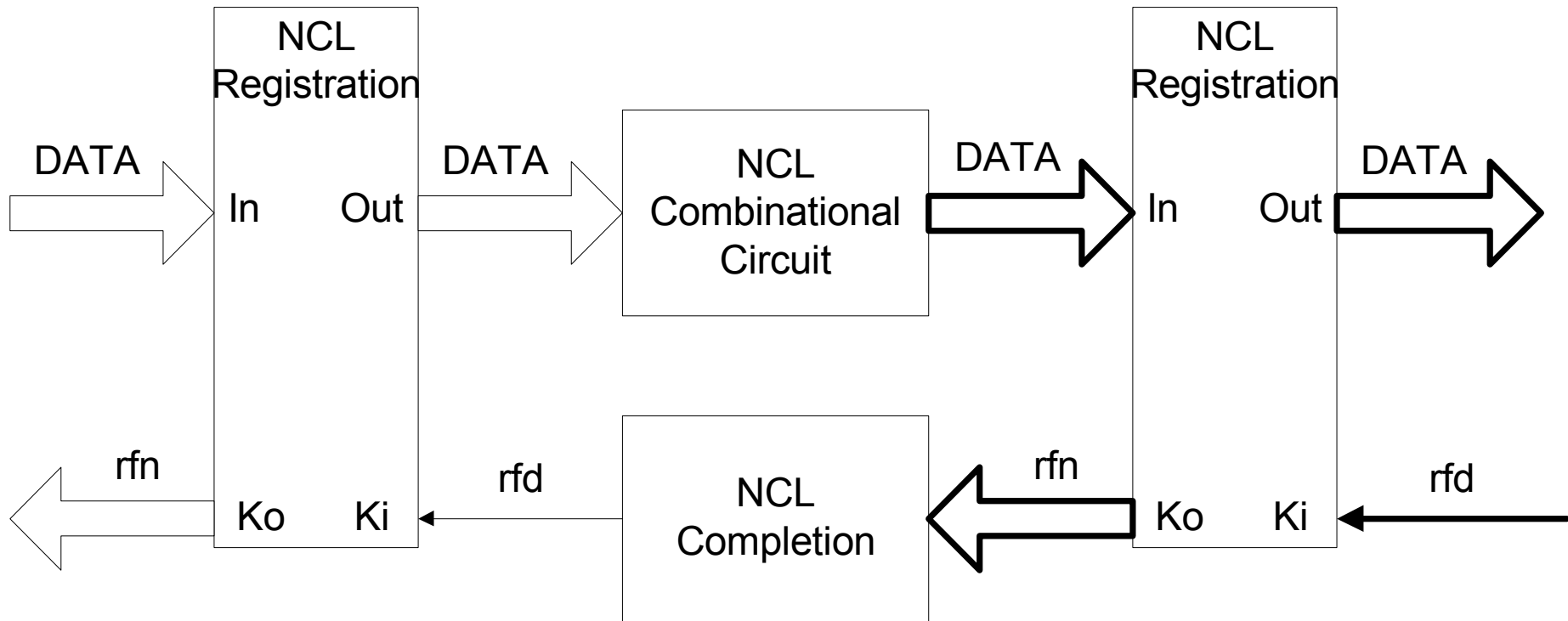
- **NULL/DATA cycle:**



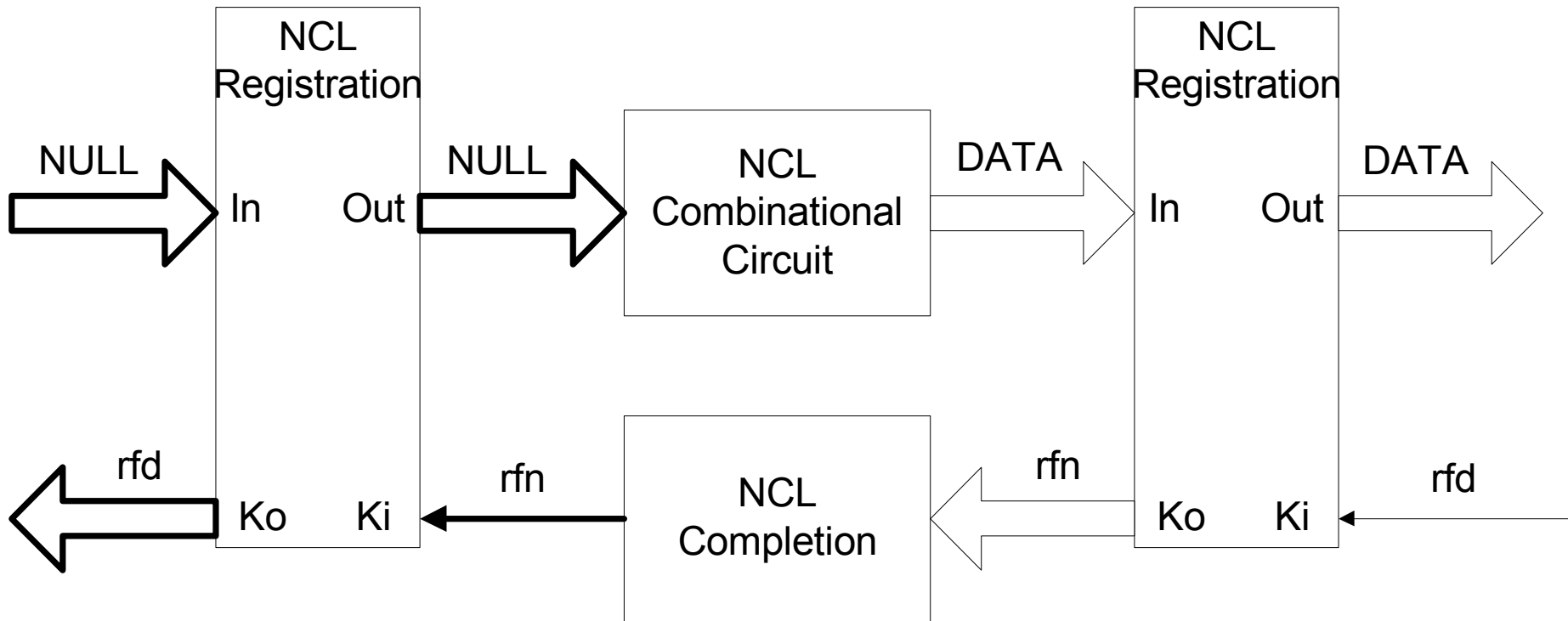
DATA Wavefront



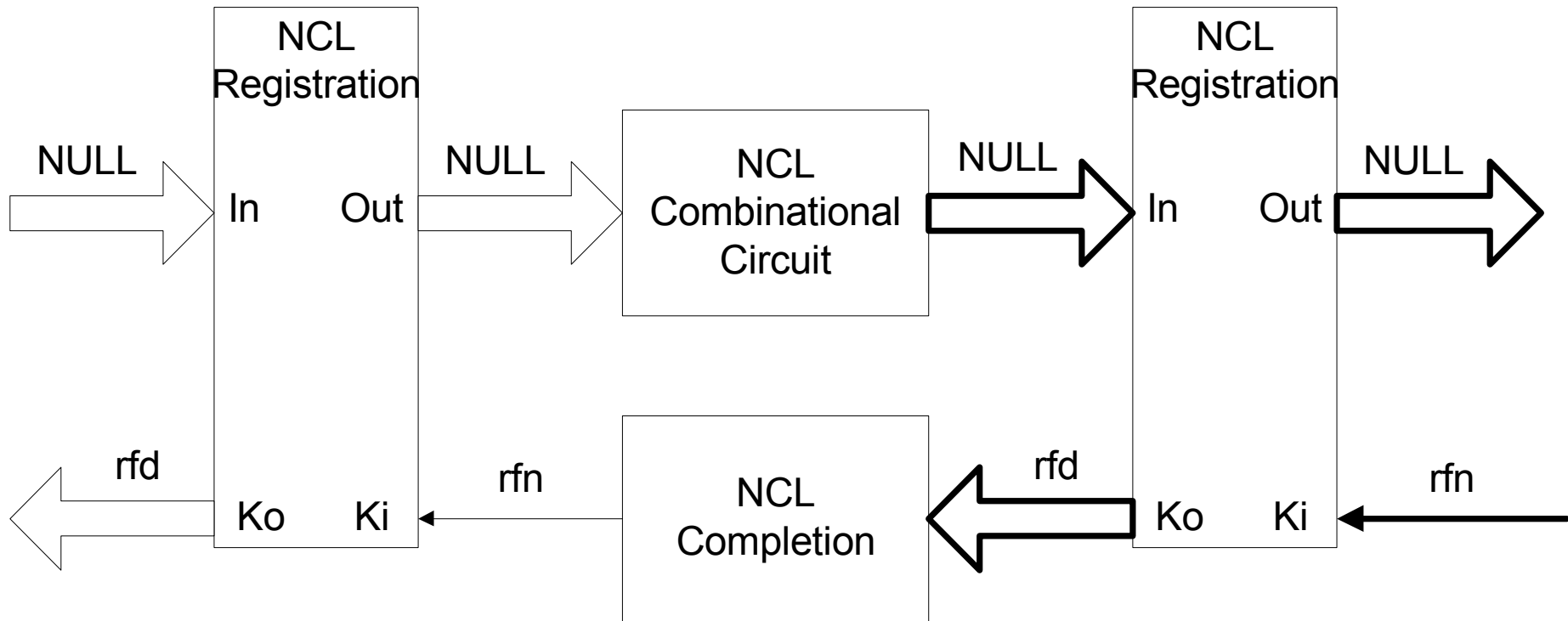
DATA Completion Detection



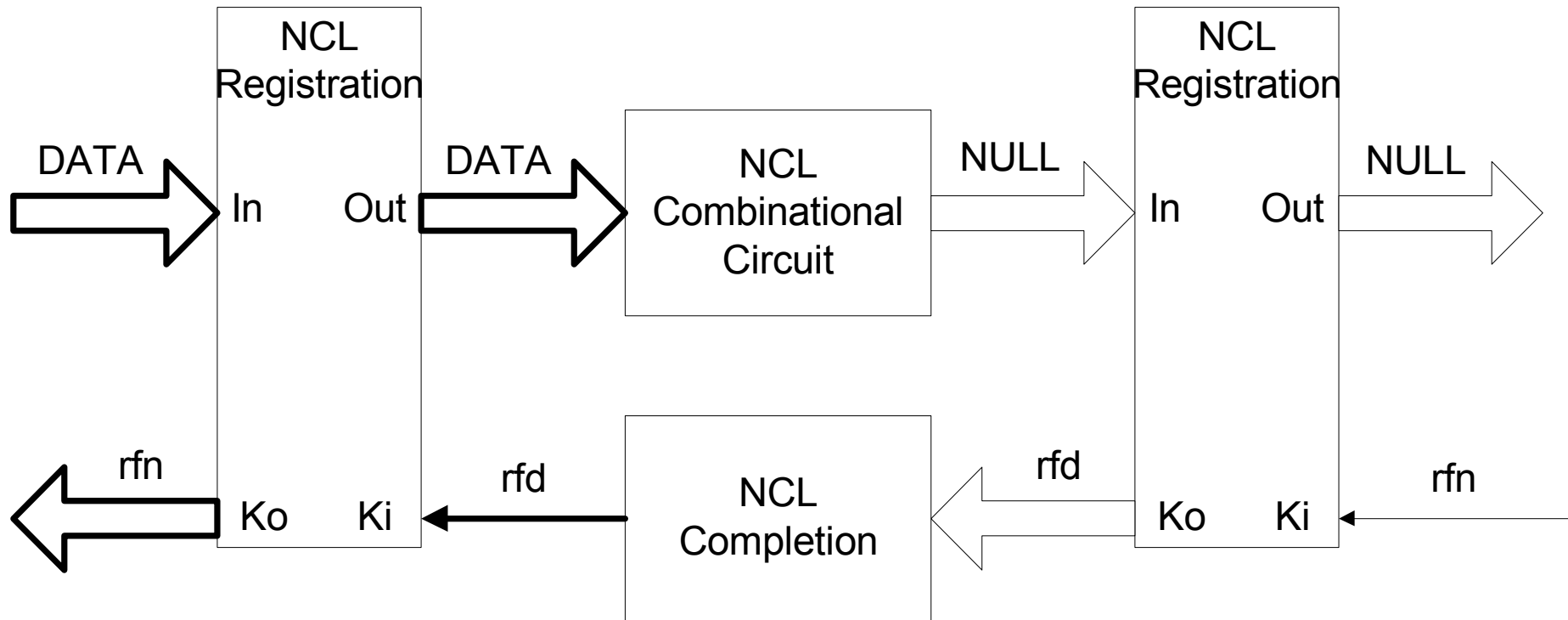
NULL Wavefront



NULL Completion Detection

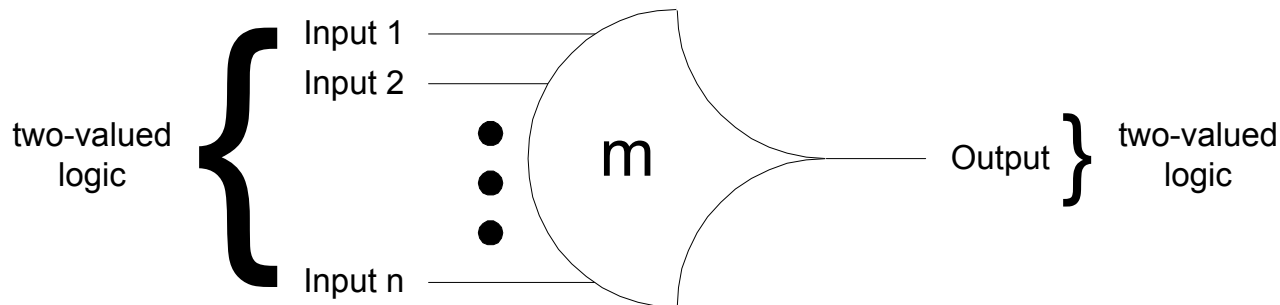


DATA Wavefront



NCL Threshold Gate

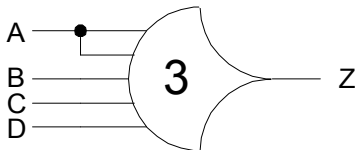
- Denoted TH m n
- Output asserted when at least m of n inputs asserted ($1 \leq m \leq n$)
- Output hysteresis behavior
 - once output becomes asserted, it remains asserted until all inputs are de-asserted



NCL Weighted Threshold Gate

- Denoted $TH_{mn}Ww_1w_2\dots w_R$
- $m > 1$ is the gate's threshold
- n is the number of inputs
- integer value, $m \geq w_R > 1$, applied to *input* R
($1 \leq R < n$)
- Output asserted when threshold met or exceeded
- Output hysteresis behavior

TH34W2



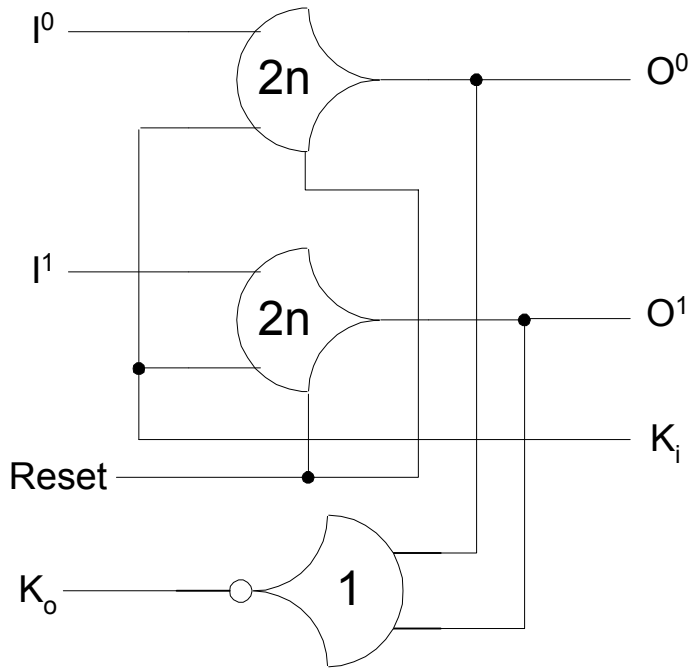
$$Z = AB + AC + AD + BCD$$

27 NCL Gates

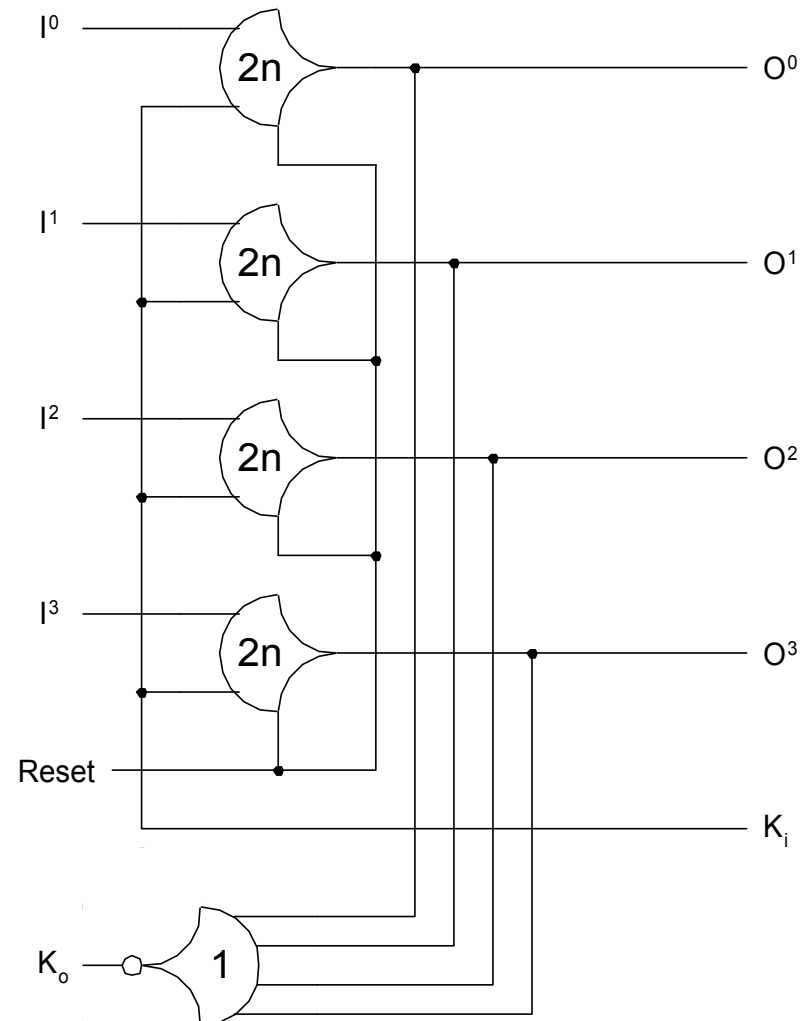
NCL Gate	Boolean Function
TH12	$A + B$
TH22	AB
TH13	$A + B + C$
TH23	$AB + AC + BC$
TH33	ABC
TH23w2	$A + BC$
TH33w2	$AB + AC$
TH14	$A + B + C + D$
TH24	$AB + AC + AD + BC + BD + CD$
TH34	$ABC + ABD + ACD + BCD$
TH44	$ABCD$
TH24w2	$A + BC + BD + CD$
TH34w2	$AB + AC + AD + BCD$
TH44w2	$ABC + ABD + ACD$
TH34w3	$A + BCD$
TH44w3	$AB + AC + AD$
TH24w22	$A + B + CD$
TH34w22	$AB + AC + AD + BC + BD$
TH44w22	$AB + ACD + BCD$
TH54w22	$ABC + ABD$
TH34w32	$A + BC + BD$
TH54w32	$AB + ACD$
TH44w322	$AB + AC + AD + BC$
TH54w322	$AB + AC + BCD$
THxor0	$AB + CD$
THand0	$AB + BC + AD$
TH24comp	$AC + BC + AD + BD$

NCL Registration

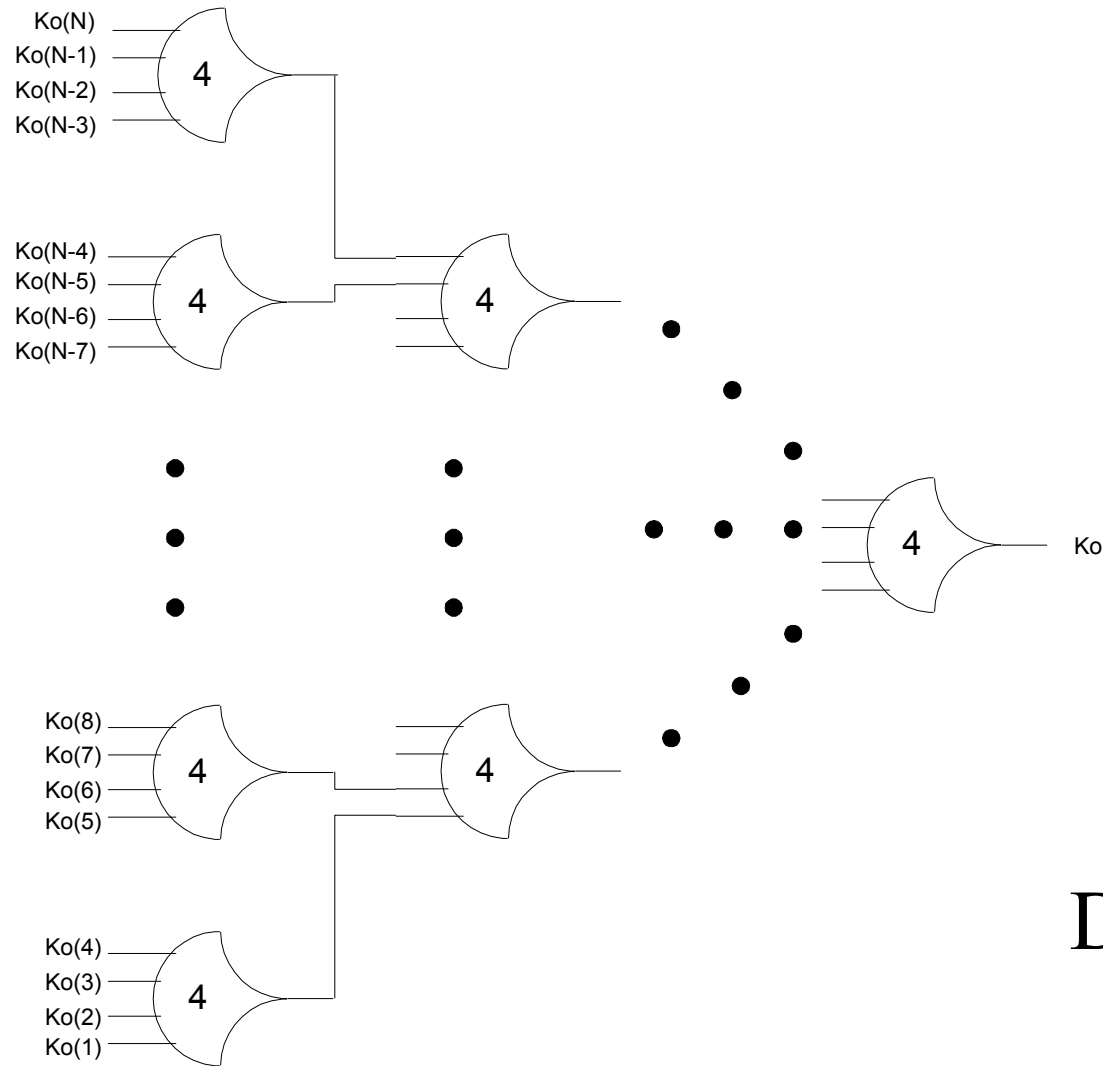
Dual-Rail Register



Quad-Rail Register



NCL Completion



$$D_{\text{comp}} = \lceil \log_4 N \rceil$$