



Integrating Asynchronous Digital Design into the Undergraduate Computer Engineering Curriculum Throughout the Nation

DUE 0717572 and 0717767

Scott C. Smith and Jia Di

Departments of Electrical Engineering and Computer Science & Computer Engineering, University of Arkansas



UNIVERSITY OF ARKANSAS
COLLEGE OF ENGINEERING

http://comp.uark.edu/~smithsco/CCLI_async.html

Project Objectives

- Improve educational practices and student learning through development of materials that provide for easy integration of asynchronous concepts into existing course structures
 - Develop lecture notes, example problems, and group projects to introduce asynchronous paradigms
- Develop a VHDL library of fundamental asynchronous gates and components
 - Develop static and semi-static transistor-level libraries of fundamental asynchronous gates
 - Develop static and semi-static physical-level libraries of fundamental asynchronous gates
 - Develop a Design-For-Test (DFT) library of fundamental asynchronous gates
- Develop NCL design and optimization CAD tools
 - Develop an asynchronous FPGA
- Integrate the developed materials into undergraduate-level courses at University of Arkansas, Missouri University of Science and Technology, and other institutions
 - Broadly disseminate the developed materials to faculty members at other institutions
- The developed materials will integrate cutting-edge technology into standard educational practices, to provide a low-cost, innovative addition to the Computer Engineering curriculum

Motivation for using Asynchronous Circuits

- Asynchronous Advantages vs. Synchronous
 - no global clock
 - lower power
 - less noise
 - less Electromagnetic Interference (EMI)
- International Technology Roadmap for Semiconductors (ITRS) predicts likely shift from synchronous to asynchronous design styles
 - increase circuit robustness
 - decrease power
 - alleviate many clock-related issues
- ITRS Data
 - shows asynchronous circuits accounted for 11% of chip area in 2008, compared to 7% in 2007
 - estimates they will occupy 17% of the world's total IC area in 2010, 30% in 2016, and 49% in 2024
 - this is a substantial portion of the multi-billion dollar semiconductor industry
- ITRS states that "power consumption is now one of the major constraints in chip design, and ITRS has identified it as one of the top three overall challenges for the last 5 years. Leakage power consumption, including its variability, has been identified as a clear long term threat and a focus topic for design technology in the next 15 years."

Project Results

- Developed Course Modules
 - Introduction to Asynchronous Logic
 - Introduction to NULL Convention Logic (NCL)
 - Transistor-Level NCL Gate Design
 - Input-Completeness and Observability
 - Dual-Rail NCL Design
 - Quad-Rail NCL Design
 - NCL Throughput Optimization
 - NCL Low Power Design
 - Group Projects
- Developed NCL Libraries
 - VHDL Library
 - package that defines fundamental NCL data types
 - file containing fundamental NCL gates
 - file containing generic versions of standard NCL registration and completion components
 - package consisting of various functions to be used in testbenches
 - Transistor-Level and Physical-Level Libraries
 - static and semi-static NCL gate implementations
 - 1.8V, 0.18µm TSMC CMOS process
 - for both Mentor Graphics and Cadence CAD tools
- Wrote Book on Asynchronous Circuit Design
- Presented Tutorials and Workshops on Asynchronous Design

Project Dissemination and Evaluation

- Course Modules and Libraries
 - available for free download from: http://comp.uark.edu/~smithsco/CCLI_async.html
 - rated as excellent by external reviewer and student users
- Asynchronous Circuit Design Book
 - Scott C. Smith and Jia Di, "Designing Asynchronous Circuits using NULL Convention Logic (NCL)," Synthesis Lectures on Digital Circuits and Systems, Vol. 4/1, July 2009
 - published by Morgan & Claypool Publishers so that it is available online for free from universities that purchase the Morgan & Claypool series
 - being utilized in multiple universities for teaching both undergraduate and graduate students
- Tutorials and Workshops
 - presented at both educational and technical conferences
 - IEEE Midwest Symposium on Circuits and Systems, July 2010
 - International Conference on Microelectronic Systems Education, July 2009
 - World Congress in Computer Science, Computer Engineering, and Applied Computing, July 2008
 - IEEE Region 5 Technical Conference, April 2007
 - 3-Day Faculty Workshops at University of Arkansas
 - 10 participants from 8 universities in summer 2009
 - 9 participants from 8 universities in summer 2008
 - rated as excellent by attendees

Asynchronous Circuit Design Book

- Scott C. Smith and Jia Di, *Designing Asynchronous Circuits using NULL Convention Logic (NCL)*, Synthesis Lectures on Digital Circuits and Systems, Vol. 4/1, July 2009, Morgan & Claypool Publishers
- 1. Introduction to Asynchronous Logic
- 2. Overview of NULL Convention Logic (NCL)
 - 2.1 NCL System Framework and Fundamental Components
 - 2.2 Transistor-Level NCL Gate Design
- 3. Combinational NCL Circuit Design
 - 3.1 Input-Completeness and Observability
 - 3.2 Dual-Rail NCL Design
 - 3.3 Quad-Rail NCL Design
- 4. Sequential NCL Circuit Design
 - 4.1 NCL Implementation of Mealy and Moore Machines
 - 4.2 NCL Implementation of Algorithmic State Machines
- 5. NCL Throughput Optimization
 - 5.1 Pipelining
 - 5.2 Embedded Registration
 - 5.3 Early Completion
 - 5.4 NULL Cycle Reduction
- 6. Low-Power NCL Design
 - 6.1 Wavefront Steering
 - 6.2 Multi-Threshold CMOS (MTCMOS) for NCL (MTNCL)
 - 6.2.1 MTCMOS for Synchronous Circuits
 - 6.2.2 Implementing MTCMOS in NCL Circuits
- 7. Comprehensive NCL Design Example

10) File I/O

HW#5: augment the Design Project #1 testbench to read the inputs from a text file and store the outputs to a text file

11) Overview of Asynchronous Logic

12) Overview of NCL

13) Input-Completeness and Observability

14) NCL Dual-Rail Combinational Logic Design

15) NCL Pipelining Optimization

HW#6: NCL assignment

16) Asynchronous Circuit Synthesis

Design Project #2: design NCL generic arithmetic circuit, such as a MAC, iterative divider, greatest common divisor (GCD), etc.

VHDL Course Modifications

- senior/graduate-level elective course
- 3 weeks of original topics replaced by 2 2/3 weeks of asynchronous logic topics
- changes do not eliminate any key VHDL course modules
- 1) Introduction to Modeling with VHDL
- 2) Entity and Architecture Statements
- 3) Test Benches
- 4) Basic UNIX commands and Mentor Graphics VHDL compiler and simulator
 - HW#1: design simple behavioral, dataflow, and structural models and testbench
- 5) Packages, functions, and procedures
 - HW#2: write a package including functions and procedures
- 6) Mealy and Moore machines
 - HW#3: Mealy and Moore machines, including design, VHDL behavioral and dataflow implementation, state minimization, and state assignment
- 7) Algorithmic State Machines (ASMs)
- 8) Mentor Graphics VHDL synthesis tool
 - HW#4: ASM throughput capability (TPC) calculation, TPC optimization, and VHDL dataflow implementation and synthesis
- Design Project #1: design complex chip, such as Run-Length Encoder, Huffman Decoder, etc.

Midterm Exam

9) Generic Constants and Generate Statements

HW#5: design a generic Multiply and Accumulate unit (MAC)

10) File I/O

11) Floating-Point Arithmetic

HW#6: design IEEE single precision floating-point coprocessor

12) Simple RISC Microcontroller Architecture

Design Project #2: augment RISC architecture discussed in class to include additional instructions, such as various branches, a NOP, and a compare, and implement in VHDL, including Text I/O in testbench

13) Overview of Verilog Modeling Language

Final Exam

Developed Low Power Digital Systems Course

- Introduction
 - 1.1 Why Low Power?
 - 1.2 Power and Energy Metrics
- Power Consumption in CMOS Digital Circuits
 - 2.1 Review of MOS Transistor Behavior
 - 2.2 Dynamic Power Consumption
 - 2.3 Short Circuit Power Consumption
 - 2.4 Leakage Power Consumption
 - 2.5 Change of Design Philosophy
- Circuit-Level Power Reduction Techniques
 - 3.1 Supply/Threshold Voltage Scaling
 - 3.2 Multiple V_{DD}
 - 3.3 Transistor Sizing and Technology Mapping
 - 3.4 Review of Combinational CMOS Logic
 - 3.5 Transistor Reordering
- Logic- and Architecture-Level Power Reduction Techniques
 - 4.1 Concurrency
 - 4.2 Pipelining and Clock Gating
 - 4.3 Power-Aware Design
 - 4.4 Pipeline Gating for Power Awareness
 - 4.5 Glitch and Reduction
- Algorithm- and System-Level Power Reduction Techniques
 - 5.1 Review of Numbering Systems
 - 5.2 Data Representation
 - 5.3 Pre-Computation
 - 5.4 Concurrency Revisited
- Ultra-Low Power Technology
 - 6.1 Leakage Control in Stand-by Mode
 - 6.2 Leakage Control in Active Mode
 - 6.3 Optimal Operating Voltages for Subthreshold Operation
 - 6.4 Subthreshold Cell Design
- Asynchronous Logic for Low Power
 - 7.1 Introduction to Asynchronous Logic
 - 7.2 Basic Concept of Asynchronous Logic Design
 - 7.3 Asynchronous Circuit Design for Ultra-Low Power
- Design Considerations for Power Efficient Applications
 - 8.1 Creating a System Definition
 - 8.2 Designing the Embedded System
 - 8.3 Energy Harvesting for No-Power Embedded Systems

VLSI Course Modifications

- senior/graduate-level elective course
- asynchronous logic topics incorporated by replacing previous miscellaneous lecture topics, by replacing Lab#4's flip-flop layout with layout of static and semi-static NCL gates, and by utilizing NCL circuits for the semester's comprehensive design project
- 1) Introduction to VLSI Systems
 - Lab#1: VHDL coding, synthesis, and simulation
- 2) CMOS Transistor Theory
- 3) Fabrication, Layout, and Design Rules
 - Lab#2: gate-level and transistor-level schematics and simulation
- 4) Analysis of Static Inverter
 - Lab#3: layout of static inverter and RC extraction
- 5) Design and Optimization of Static CMOS Gates
- 6) Introduction to NCL
- 7) Transistor-Level Design of NCL Gates
- 8) Critical Path Delay Analysis and Transistor Sizing
- 9) Dynamic CMOS Circuit Design
 - Lab#4: layout of basic static Boolean gates and static and semi-static NCL gates (NCL gates replaced flip-flops)
- 11) Static Timing Analysis for Sequential Circuits
- 12) Low Power Design
 - Lab#5: schematic driven layout
- 13) Datapath Design for Synchronous Circuits (e.g., comparators, adders, multipliers, registers, etc.)
- 14) Datapath Design for NCL Circuits (e.g., registration, completion, and DR and QR combinational circuits)
- Lab#6: synchronous datapath design and simulation
- 15) Semiconductor Memories
- 16) Clock Distribution, PLL, Clock Skew, and Jitter
- 17) Floorplanning, Placement, and Routing
- 18) Control Unit Design
- 19) VLSI Testing and Design for Test
 - Design Project: design, layout, and simulate various NCL arithmetic circuits (e.g., quad-rail unsigned 24+8x8 MAC, dual-rail 2s Complement 8x8 Booth2 multiplier, and dual-rail 2s complement 8x8 Baugh-Wooley multiplier)
- 20) Future Trends in VLSI Design