

Delay-Insensitive Asynchronous ALU for Cryogenic Temperature Environments

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Abstract— This paper details the design and performance of a delay-insensitive asynchronous 8-bit ALU for an asynchronous 8051-compliant microcontroller intended for extreme environments. The ALU was designed using a quasi-delay-insensitive logic called NULL Convention Logic (NCL), in order to allow for reliable circuit operation over a wide temperature range and enable extreme supply voltage scaling for low power consumption. The ALU was fabricated along with several other 8051-essential components at MOSIS using the IBM SiGe5AM 0.5 μm process. A series of tests at both room and cryogenic temperatures has been performed, which has demonstrated that the designed ALU is able to operate correctly from 2K (-271 °C) to 297K (23 °C), as well as over wide supply voltage variations.

I. INTRODUCTION

An ALU is a necessary component of any general-purpose microcontroller/microprocessor. Therefore, reliability of such a system relies heavily on the performance of the ALU. Currently, most digital circuits are designed using a synchronous approach, which results in chips requiring precise timing of their components. Functionality problems arise when such circuitry is placed in extreme environments with temperatures ranging from room temperature to -270°C, due to the variances in semiconductor device behaviors. To remedy this, the local environment surrounding the circuitry can be altered to match its operational requirements (warm box) or the design of the circuitry can be changed to eliminate the timing dependencies. NULL Convention Logic (NCL) [1] was chosen as the design logic for this ALU, as it is a delay-insensitive asynchronous logic that effectively eliminates such timing dependencies, allowing the design to match the specification while operating under extreme environments. Additionally, SiGe was chosen due to its compatibility with standard silicon processing techniques and its operability over desired temperature ranges [2-3].

II. DELAY-INSENSITIVE ASYNCHRONOUS CIRCUITS AND NULL CONVENTION LOGIC

Recently, asynchronous logic has drawn more attention. One of the major reasons is the clock management problem for the increasingly complex synchronous circuits. Delay-insensitive asynchronous logic uses handshaking protocols rather than clocks to control the circuit behavior. Theoretically,

delay-insensitive circuits have the ability to function correctly as long as the transistors can switch properly [4].

NULL Convention Logic (NCL), a quasi-delay-insensitive logic, is a symbolically complete logic, which expresses process completely in terms of the logic itself. Logic signals in NCL circuits are usually encoded in a multiple-rail format. The simplest encoding scheme is dual-rail logic, which uses two wires to interpret one signal value. There are two valid states: DATA state, which including DATA 0 and DATA 1, and NULL, represented by both wires being logic low. The NCL logic family is composed of threshold gates. An m -threshold, n -input threshold gate is denoted as TH m_n , where the output is asserted when at least m of the n inputs are logic high. Because NCL threshold gates are designed with hysteresis, once the output is asserted, it remains asserted until all n inputs are logic low. The operation of NCL circuits includes DATA-NULL cycles: after a DATA state, all signals in a stage go to a NULL state before the next DATA state. This DATA-NULL cycle operation, together with the hysteresis property of threshold gates, fits the needs of a feedback request/acknowledge signal based handshaking protocol, which eliminates the effect of gate delay on circuit function, making NCL circuits speed-independent.

The general NCL circuit architecture consists of pipeline stages with combinational logic, asynchronous registers/latches, and completion detection circuitry. Two adjacent register stages interact through their request and acknowledge signals, K_i and K_o , respectively, to prevent the current DATA wavefront from overwriting the previous DATA wavefront, by ensuring that the two DATA wavefronts are always separated by a NULL wavefront. The acknowledge signals are combined in the Completion Detection circuitry to produce the request signal(s) to the previous register stage. When all current register outputs are DATA, the corresponding completion detection signal will be logic 0, indicating a “request-for-NULL”; and when all current register outputs are NULL, the corresponding completion detection signal will be logic 1, indicating a “request-for-DATA”. After receiving the request signal, the previous register will allow the corresponding NULL/DATA wavefront to pass to the combinational logic block between the two registers.

III. ALU

A. Design

The design of the ALU is similar to its Boolean counterpart, since it is a purely combinational circuit. As such, the gate composition of the entire ALU was designed using the Threshold Combinational Reduction (TCR) methodology [5]. The control signals of the ALU direct the operands to only the appropriate logic for that operation. The results of all operations are ORed together to generate the output, which can be done because for any given DATA cycle, only the output of the desired operation is calculated; the others are NULL. The ALU is capable of executing the following arithmetic operations: add, addc, subb, inc, dec, inc DPTR, mul, div, and DA. It is also capable of executing the following logical operations: and, or, xor, CPL, RL, RR, RLC, RRC, and swap. A complete definition of each instruction can be found in the 8051 user manual [6]. Due to pin limitations of the package, shift registers were added on the inputs and outputs to reduce the total pin count of the chip, an addition that required some extra control logic for proper operation. Figure 1 shows a block diagram of the ALU with shift registers.

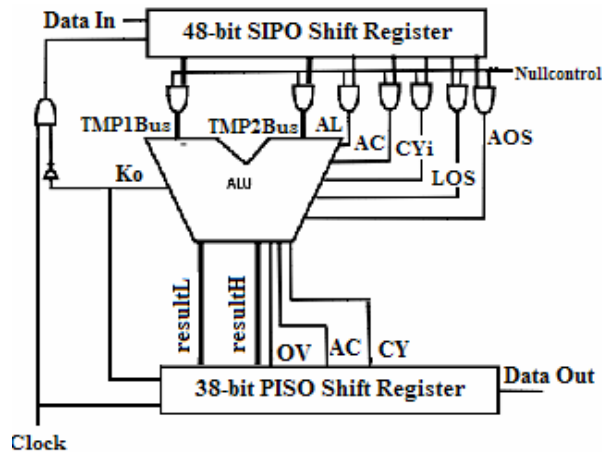


Figure 1. ALU Block Diagram

In order to pass a DATA set to the ALU, the signal Nullcontrol must first be driven low. While Nullcontrol is low, all inputs to the ALU are low, effectively representing a NULL set. Once the NULL set has passed through the ALU to the outputs, the signal Ko will go low. While Ko is low, the clock signal gets passed to the input shift register allowing for data to be shifted into it. Once a DATA set has been shifted into the input shift register, Nullcontrol is driven high. This allows the DATA set to propagate through to the ALU. Once the ALU has received a complete DATA set, Ko will go high. Ko is used in the output shift register to select which data to pass through a flip-flop, an output of the ALU or the output of the previous flip-flop. Once the signal Ko goes high, the clock to the input shift register is disabled, and after two clocks, the

outputs of the ALU can be shifted out. Figure 2 shows a picture of the fabricated die with ALU highlighted which has a layout size of $1.5\mu\text{m}\times 1.5\mu\text{m}$.

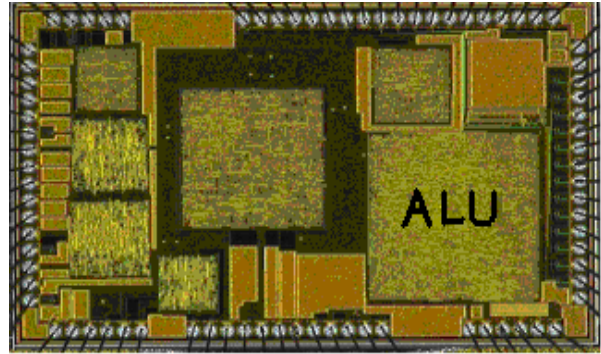


Figure 2. ALU on die

B. Testing Setup

In addition to room temperature testing (described next), the ALU was cryogenically tested using a setup comprised of a custom built cryostat, pattern generator (PG3A), logic analyzer (TLA5024B), oscilloscope, variable power supply, temperature control, and a voltmeter. The cryostat is composed of an insulating outer shell that encases a vertical series of plates whose centers are connected by a metal rod. The IC to be tested is mounted on the bottom side of the lowest plate. Ribbon cable connected to the IC runs up through the series of plates to the top of the chamber where they are attached to connectors. The connectors are connected to a custom test board which interfaces with the rest of the hardware. The pattern generator is connected to the inputs of the test board. Outputs from the test board are connected to the logic analyzer or the oscilloscopes depending on the data being measured and the exhaustiveness of the test. The ALU output is connected in series with a 20Ω current sensing resistor via the test board. The voltmeter probes each side of the resistor to measure the voltage across it. A picture of the test setup is shown in Figure 3.

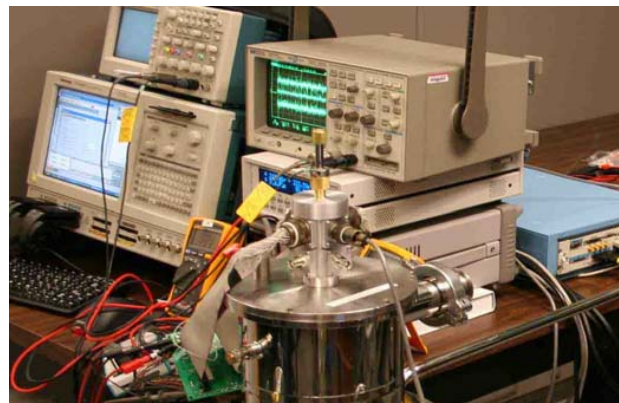


Figure 3. Cryogenic Test Setup

The initial room temperature setup involved a similar setup without the cryostat. The main difference between the two setups is the distance between the test board and the IC. In the room temperature test setup, the IC is placed a minimal distance from the test board. In the cryogenic test setup, the IC is connected to the test board by around 1 meter of wire. This drastically affected the noise observed between the two setups.

C Testing Procedure

For cryogenic testing, helium is pumped into the cryostat and begins entering from the bottom of the chamber via a nozzle located below the mounted IC. The helium immediately comes into contact with the first of two heating sensors which works in conjunction with the temperature control unit to maintain a specified temperature. The other heating sensor is located at the top of the plate with the mounted IC. The temperature of this sensor was used in recording all measurements across temperature.

For early test runs, it was important to test not only the functionality of the circuit, but its voltage scaling tolerance as well. As such, the minimum operating voltage of the ALU was tested across a range of frequencies. This was the lowest supply voltage that the ALU could execute a particular instruction's DATA and NULL cycle at a given frequency, which includes the shifting in and out of data at that frequency. The instruction chosen was viewed at room temperature to require a higher voltage than all other viewed instructions. At this voltage, it is assumed that the ALU is consuming the least amount of power for that operating frequency and temperature. As such, power was calculated at minimum supply voltages by using the voltage measured across the current sensing resistor. This procedure was used in later tests, whose main focus was measuring the effect of voltage/temperature scaling on the power of the circuit.

For the initial cryogenic test run, minimum supply voltage and power were measured across a range of temperature points. Voltage results can be viewed in Figure 4. A second cryogenic test run was performed to make a more conclusive measurement of voltage and power over temperature. In order to do that, the ALU was tested at only two frequencies as temperature was continuously lowered. The values measured matched those in the first cryogenic test run. Voltage results of that run can be seen in Figure 5. A third cryogenic test run was performed to determine more accurately the effect of voltage/temperature scaling on power. For that run, power was measured across a range of well-known operating voltages while the circuit ran at a constant frequency. Results from that run can be viewed in Figure 6.

For the room temperature tests, only the minimum supply voltage was measured across a range of frequencies. Results can be seen in Figure 7.

IV. RESULTS

Experimental results show that the designed ALU is able to function correctly over a wide temperature range from 2K (-271 °C) to room temperature 300K (23 °C), as well as sustain extreme supply voltage scaling to as low as 0.36V for low power.

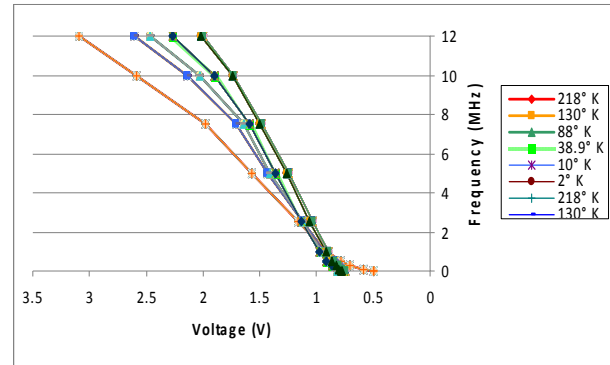


Figure 4. Minimum Supply Voltage per Operating Frequency over Temperature

The voltage results of the first cryogenic test run matched well with expected results. As the operating frequency was lowered, the minimum supply voltage required to sustain functionality also lowered. This trend, for the most part, maintained itself across temperature. While this trend maintained itself when compared to the power measurements, the values obtained were larger than expected. One possible reason could be the longer wires came out of the cryostat that the chip was driving..

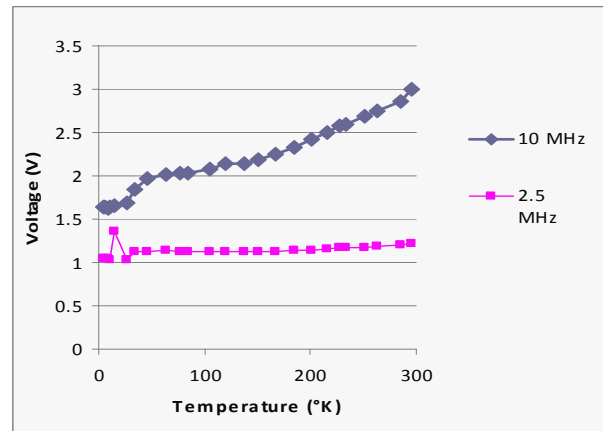


Figure 5. Minimum Supply Voltage over Continuous Temperature Decrease

The results in the second cryogenic test run directly corresponded to the results obtained from the first test run. Minimum supply voltage more or less decreased linearly as temperature was lowered, but the same values of power were still observed.

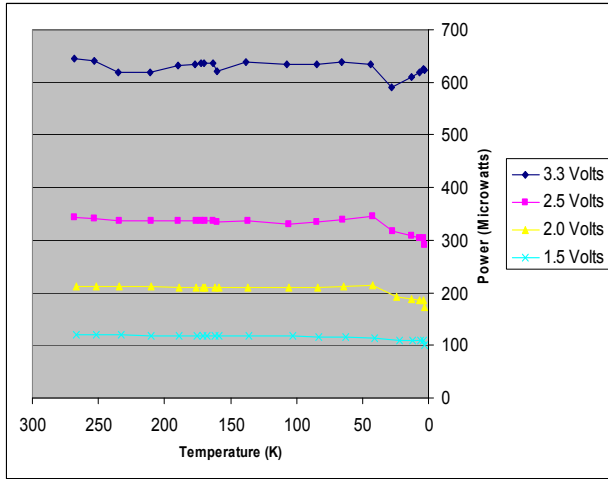


Figure 6. Power Consumption at 2.5MHz

The results of the third cryogenic test run, matched expected power results more closely. As voltage was scaled down, a somewhat exponential decrease in power occurred. From 270K to around 65K, power was decreasing at a steady pace, while the largest decreases were observed at temperatures at or below roughly 40K, with decreases as large as 18.6%. At this point it is important to note that measurements obtained with the cryogenic test setup were noisier than those taken with the room temperature test setup. Noted from Figure 8, the ALU was capable of operation at much lower voltages (0.36 V was the lowest supply voltage measured) when at room temperature with a cleaner input signal.

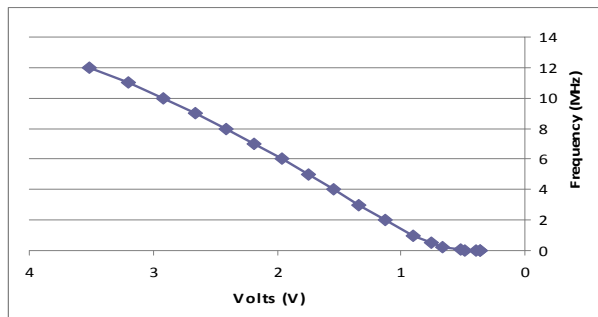


Figure 8. Minimum Supply Voltage per Operating Frequency at 23° C

V. CONCLUSIONS AND FUTURE WORK

In general, the measured voltages and power correlate with expected results. As the temperature of the ALU decreased, the minimum supply voltage and power consumption also decreased. In addition, the minimum supply voltage and power consumption decreased along with the operating frequency of the ALU. These results were obtained with a significant amount of noise on the input and output signals to/from the circuit, likely due to the more than one meter of wire between the input/output pins of the circuit and the test board. Therefore, it is highly likely that the ALU will operate at even lower voltages and use less power than the data obtained shows. More testing will be performed to show how much noise actually impacts the current measurements.

The room and cryogenic temperature tests have demonstrated that delay-insensitive asynchronous circuits fabricated using IBM SiGe 5AM process are able to function correctly over a wide temperature range and at extremely low temperature (2K). Future work includes applying this design methodology to more complex circuits, e.g., a full 8051-compliant microcontroller, to further explore its behavior in an extreme temperature environment.

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