

# AVINASH S. KASHYAP

1790 N. Gregg Ave #1

Fayetteville, AR 72703

Phone: (479) 236-0280

Email: akashya@uark.edu, avi.kash@gmail.com

Personal Home page: <http://comp.uark.edu/~akashya>

## OBJECTIVE:

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A double doctoral fellowship holder seeks to obtain a full-time position that harnesses his varied skills in the area of compact modeling and characterization of semiconductor devices.

## RESEARCH FOCUS:

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Device physics, operation, modeling & characterization of semiconductor devices esp., CMOS, LDMOS, SiC power semiconductor devices.

Skill set: Device modeling, Parameter extraction and optimization using IC-CAP, device analysis and design, fabrication, characterization, Taurus/Medici TCAD tools, Verilog-A, Cadence Design Suite (Spectre, Virtuoso).

## EDUCATION:

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**Ph. D. Electrical Engineering** – Summer 2009.

\* University of Arkansas, Fayetteville. **GPA: 3.9**

\* Dissertation: *Compact Cryogenic Modeling of LDMOS Devices for Extreme Environment Analog Circuit Design.*

**M. S. Electrical Engineering**

\* University of Arkansas, Fayetteville. **GPA: 3.81**

\* Thesis: *Compact Circuit Simulation Modeling of Silicon Carbide Vertical Channel Junction Field Effect Devices.*

**B. Tech. Electrical & Electronics Engineering**

\* University of Calicut, India.

## INDUSTRIAL EXPERIENCE:

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March 2009 – current:

**Device Modeling Consultant: Boeing Corporation**, Seattle, WA.

- Cryogenic modeling of **IBM's 7HP** SiGe process down to -180 °C for analog circuits in aerospace applications.
- Involved in infrastructure set-up such as installing the IBM 7HP kit and interfacing it with Spectre.
- Extracted parameters for CMOS devices of various sizes using the **BSIM3v3** model.
- Created binned models for operation in upper and lower cryogenic temperatures.

May 2006 – Sep 2006:

**Device Modeling Intern: Spice Modeling Group, National Semiconductor Corporation** – Santa Clara, CA.  
Mentor – Dr. Pascale Francis.

- Worked on implementing the industry standard **PSP MOS** model for one of National Semiconductor's advanced CMOS technologies used in power management circuitry.
- Involved in setting up the infrastructure required for using the model such as setting up IC-CAP and Spectre for Linux environment, installing SimKit etc.
- Characterization of devices using probe station, parameter analyzer etc.
- Evaluation and parameter extraction performed for DC, CV and over temperature (-50 °C to 150 °C) for the entire geometry using IC-CAP.
- Comparison of PSP model performance with that of BSIM4 model was done to analyze if National should shift to the new industry standard.
- Documented the procedure and created custom extraction routines for in-house usage.
- Presented recommendations on deploying the model for circuit design to the SPICE Modeling Group.

May 2005 – Aug 2005:

**Research Associate:** Wide bandgap research group, **Oak Ridge National Laboratory (ORNL)** – National Transportation Research Center (NTRC), Knoxville, TN. Mentor – Dr. Burak Ozpineci.

- Involved in the characterization and compact modeling of Silicon Carbide JFETs and Schottky barrier diodes used in voltage source inverters for hybrid electric vehicles.
- Deployed the compact JFET model that I developed in my thesis in real-life automotive applications.
- This was part of the Department of Energy's (DoE) FreedomCAR project. The work also involved building test benches for device characterization and system level modeling and validation of inverters.
- Conclusively proved the increase in efficiency of inverters with the use of SiC devices.
- Findings reported in DoE's annual report, journal and conference papers published.

### **ACADEMIC RESEARCH EXPERIENCE:**

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Jan 2005 - Present:

**Group Leader:** Semiconductor Device Modeling Group, University of Arkansas. Dissertation Advisor - Dr. H. Alan Mantooth

- Developed the **world's first** cryogenic LDMOS model capable of replicating carrier freeze-out.
- Circuits built with the model should operate in lunar environments (down to -180 °C). This is for NASA's upcoming Lunar mission.
- Developed cryogenic extensions to the MOS20 model from NXP semiconductor.
- Project in collaboration with the **Jet Propulsion Laboratory**, Pasadena, CA.
- Model equations modified to incorporate extreme environment operation.
- Analog circuits successfully designed with the model. The circuits are currently place aboard the International Space Station for testing.
- Findings published in major conferences and journals.
- Responsibilities as Group Leader also include managing graduate students and their research, writing proposals, conducting original research and coordinating publications within the group.
- Have also been involved in various consulting projects from time to time.

Jan 2003 – Dec 2004:

**Graduate Research Assistant:** Semiconductor Device Modeling Group, (MSCAD Lab), **University of Arkansas**, Fayetteville. Thesis Advisor - Dr. H. Alan Mantooth.

- Master's thesis - compact circuit simulation modeling of a silicon carbide static induction transistor (SIT) and JFET, using the MAST high level modeling language and simulating it using the SABER simulator.
- The work involved characterizing devices and developing models for extreme environment switching applications.
- The devices have also been modeled in VHDL-AMS using the Paragon package developed in-house.
- MEDICI simulations were used to understand the physics of the operation of the device. The model has been validated with actual device (Northrop Grumman, Infineon/SiCED) measurements.
- Collaborators included NIST, Northrop-Grumman, NASA Glenn and Cree Research.
- First ever unified physics based simulation model for a SiC SIT and JFET.

### **AWARDS & ACCOLADES:**

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\* Awarded the prestigious **Sam Walton Doctoral Academy Fellowship** for four years (2005-2009) to pursue Ph. D. at the University of Arkansas. It is awarded to Doctoral students with the highest academic and research credentials.

\* Awarded the **William E. Clark Endowed Doctoral Fellowship**. These two fellowships are in addition to the research assistantship awarded by the department.

\* Awarded the University of Arkansas graduate student travel grant for the years 2003, 2004, 2005 and 2008 to present research papers in international conferences.

\* Research work and lab featured in the Arkansas Democrat Gazette (dated 9/12/05), the state's main newspaper.

\* Awarded the State Government of Kerala Merit scholarship for academic excellence (1997-2001). Undergraduate tuition and expenses were fully sponsored by the Government.

\* Awarded second place in the annual co-op symposium at Arkansas.

\* Placed in the top 0.2% among 57,000 students in the Kerala State engineering entrance examination in India.

\* Unanimously elected as the President of the electrical engineering association in college, representing a student body in excess of 400.

## **LABORATORY EXPERIENCE:**

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Signatone probe station, Keithley 4200 Parameter Analyzer, HP precision LCR meter (4284A), Tektronix 371B curve tracer, optiprobe, scanning electron microscope (Hitachi), MBE & PECVD equipment, ATE tester, Electroplating (Au, Ni), reactive ion etcher, sputtering (XM-8), four point probe, HP impedance analyzer, ICP etcher, Evaporator, profilometer, oxidation equipment, dicing, wire bonding.

## **COMPUTER SKILL SET:**

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Operating Systems: Windows, Unix/Linux  
HDL: MAST, VHDL-AMS, Verilog-A  
Packages: IC-CAP, complete Cadence ICFB suite (Spectre, Virtuoso, Analog environment etc), MEDICI, Mentor Graphics IC design station, SABER (Synopsys), PSPICE (OrCAD), System Vision (Mentor Graphics), Simplorer (Ansoft) T-Suprem IV, Veritas HDL, LabVIEW

## **RELEVANT COURSEWORK:**

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Analog IC design, High temperature analog IC design in silicon carbide, IC design & layout (Analog & Digital), advanced IC fabrication technology, semiconductor devices, high speed semiconductor devices, finite element modeling (MEDICI) of semiconductor devices, advanced mixed signal test engineering, mixed signal modeling & simulation, power electronics, thin film Lab, ASIC design, switch mode power conversion.

## **LANGUAGES KNOWN:**

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English, Tamil, Hindi, Malayalam, Sanskrit, French (Beginner), German (Beginner).

## **ORGANIZATIONS AND ACTIVITIES:**

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- \* Institute of Electrical and Electronics Engineers (IEEE)
- \* IEEE Power Electronics Society (PELS)
- \* International Microelectronics and Packaging Society (IMAPS)
- \* IEEE Components, Packaging, and Manufacturing Technology (CPMT)
- \* Reviewer for the IEEE Energy Conversion Congress and Exposition (ECCE) 2009
- \* Reviewer for the Power Electronics Specialists Conference 2005, 2006, 2007, 2008
- \* Reviewer for the Applied Power Electronics Conference 2006, 2007

## **PUBLICATIONS:**

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### **Thesis**

- \* **A. S. Kashyap**, "Compact Modeling of Silicon Carbide Junction Field Effect Devices," M.S. Thesis, Dept. Electrical Engineering, University of Arkansas, Fayetteville, AR, 2005.

### **Journal**

- \* **A. S. Kashyap**, H. A. Mantooh, "Characterization and Modeling of LDMOS devices for extreme environments," *IEEE Trans. Electron Devices*, in preparation.
- \* T. Funaki, J. C. Balda, J. Junghans, **A. S. Kashyap**, F. D. Barlow, H. A. Mantooh, T. Kimoto, and T. Hikiyara, "Power Conversion with SiC Devices at Extremely High Ambient Temperatures," *IEEE Transactions on Power Electronics*, Vol. 22, Issue 4, July 2007, pp. 1321 – 1329.
- \* **Kashyap A.S**, McNutt T.R, Funaki T, Mantooh H.A, "Silicon Carbide Vertical Channel Junction Field Effect Transistor implemented in the SABER simulator," *IEEE Trans. Power Electronics*, in preparation.
- \* T. Funaki, J. C. Balda, J. Junghans, **A. S. Kashyap**, F. D. Barlow, H. A. Mantooh, T. Kimoto, and T. Hikiyara, "SiC JFET dc Characteristics Under Extremely High Ambient Temperatures," *IEICE Electron. Express.*, Vol. 1, No. 17, pp.523-527.
- \* B. Ozpineci, M. Chinthavali, L. Tolbert, **A. S. Kashyap**, H. A. Mantooh, "A 55 kW Three-Phase Inverter with Si IGBTs and SiC Schottky Diodes," *IEEE Transactions on Industry Applications*, Jan 2009, pp. 278-285.

\* **A. S. Kashyap**, S. D. Magan Lal, T. R. McNutt, A.B. Lostetter & H. A. Mantooh "Testing and Modeling Electrical Characteristics of Novel Silicon Carbide (SiC) Static Induction Transistors (SITs)," *Journal of the Arkansas Academy of Sciences*, April 2003.

## Conference

\* **A.S. Kashyap**, H. A. Mantooh, T. Vo, M. Mojarradi, "Cryogenic Modeling Lateral DMOS Transistors for Lunar Applications," *IEEE Custom Integrated Circuits Conference*, 2009, Submitted.

\* **A.S. Kashyap**, M. Mudholkar, H. A. Mantooh, T. Vo, M. Mojarradi, "Cryogenic Characterization of Lateral DMOS Transistors for Lunar Applications," *IEEE Aerospace Conference*, Big Sky, MT, March 2009.

\* **A.S. Kashyap**, M. Mudholkar, H. A. Mantooh, T. Vo, M. Mojarradi, "Carrier Freeze-out Phenomenon in LDMOS Devices in Deep Cryogenic Temperatures," IPPW, Atlanta, June 2008.

\* **Kashyap A.S**, Ramavarapu P.L, Maganlal S, McNutt T.R, Lostetter A.B, Mantooh H.A, "Modeling Vertical Channel Junction Field Effect Devices in Silicon Carbide," *Conf. Rec. of IEEE Power Electronics Specialists Conf (PESC)*, Aachen, Germany, June 20-25 2004.

\* **Kashyap A.S**, Ramavarapu P.L, Maganlal S, McNutt T.R, Lostetter A.B, Mantooh H.A, "Compact Circuit Simulation Model of a Silicon Carbide Junction Field Effect Transistor," *IEEE Workshop on Computers in Power Electronics (COMPEL '04)*, Urbana-Champaign, Aug 15-18 2004.

\* **Kashyap A.S**, Vemulapally C, Mantooh H.A, "VHDL-AMS Modeling of Silicon Carbide Power Semiconductor Devices," *IEEE Workshop on Computers in Power Electronics (COMPEL '04)*, Urbana-Champaign, Aug 15-18 2004.

\* **Kashyap A.S**, McNutt T.R, Funaki T, Mantooh H.A, "High Temperature Characterization and Compact Modeling of Silicon Carbide Junction Field Effect Transistors," *IEEE India International Conference on Power Electronics (IICPE '04)*, Mumbai, India, Dec 20-21 2004.

\* T. Funaki, **A. S. Kashyap**, P. Ramavarapu, S. Maganlal, J. C. Balda, H. A. Mantooh, T. Kimoto, and T. Hikihara, "Characterization of Cascode SiC JFET / Si MOSFET Devices," *IEEE International Power Electronics Conference 2005 (IPEC '05)*, Niigata, Japan, April 4-8 2005.

\* T. Funaki, J. C. Balda, J. Junghans, **A. S. Kashyap**, F. D. Barlow, H. A. Mantooh, T. Kimoto, and T. Hikihara, "Power Conversion with SiC Devices at Extremely High Ambient Temperatures," *IEEE Power Electronics Specialists Conference*, Recife, Brazil, June 2005.

\* T. Funaki, **A. S. Kashyap**, H. A. Mantooh, J. C. Balda, F. D. Barlow, T. Kimoto and T. Hikihara, "Characterization of SiC diodes in extremely high temperature ambient," *IEEE Applied Power Electronics Conference (APEC)*, Dallas, TX, March 2006.

\* B. Ozpineci, M. Chinthavali, **A. S. Kashyap**, L. Tolbert, "A 55 kW Three-Phase Inverter with Si IGBTs and SiC Schottky Diodes," *IEEE Applied Power Electronics Conference (APEC)*, Dallas, TX, March 2006.

\* T. Funaki, **A. S. Kashyap**, H. A. Mantooh, J. C. Balda, F. D. Barlow, T. Kimoto and T. Hikihara, "Characterization of SiC JFET for Temperature Dependent Device Modeling," *IEEE Power Electronics Specialists Conference*, Jeju, South Korea, June 2006.

\* **Avinash S. Kashyap**, Sharmila D. Magan Lal, Ty R. McNutt, Alexander B. Lostetter & H. Alan Mantooh "Testing and Modeling Electrical Characteristics of Novel Silicon Carbide (SiC) Static Induction Transistors (SITs)," *Proceedings of the Arkansas Tech Summit*, April 2003.

\* **Avinash S. Kashyap**, "Hybrid Fuel Cell Gas Turbine Power Plant, with quasi zero emissions utilizing Sewage gas," *National Renewable Energy Conference 2000(NREC 2K)*, Indian Institute of Technology, Bombay, Nov 30 – Dec 2, 2000.

### **Invited Talks**

\* **A. S. Kashyap**, B. Ozpineci, H. A. Mantooth, "Silicon Carbide Device and System Modeling with MAST and SABER," *Synopsys User Group Conference*, 25 slides, Detroit, MI, Sept. 2005.

### **Non-refereed technical publications and presentations**

\* B. Ozpineci, M. S. Chinthavali, L. M Tolbert, **A. S. Kashyap**, "Wide-Bandgap Semiconductors," Department of Energy, FreedomCAR and Vehicle Technologies, Washington DC, Nov. 2005.

\* **A. S. Kashyap**, B. Ozpineci, H. A. Mantooth, "Characterization and Modeling of Silicon Carbide Devices and Systems for Hybrid Electric Vehicle Applications," Poster presentation at the Co-op Symposium, University of Arkansas, Oct. 2005. **Best poster award (2<sup>nd</sup> place).**

### **REFERENCES:**

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#### **Dr. Alan Mantooth**

Professor  
21st Century Chair in Mixed-Signal IC  
Design and CAD  
Department of Electrical Engineering  
University of Arkansas  
Fayetteville, AR 72701  
E-mail: mantooth@uark.edu  
Phone: (479) 575-4838  
Fax: (479) 575-7967

#### **Dr. Pascale Francis**

Senior Device Engineering  
Manager  
Spice Modeling Group  
National Semiconductor  
Santa Clara, CA 95051  
E-mail: Pascale.Francis@nsc.com

#### **Dr. Burak Ozpineci**

Oak Ridge National Laboratory  
2360, Cherahala Blvd,  
Knoxville, TN 37923  
E-mail: ozpinecib@ornl.gov  
Phone: (865) 946-1329  
Fax: (865) 946-1262

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